CMS80F231x User Manual

Enhanced flash memory 8-bit 1T 8051 microcontroller

Rev. 1.1.3

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1. PRODUCT OVERVIEW

1.1 Features

- **Compatible with MCS-51 1T command system**
  - The system clock frequency supports up to 48MHz
  - The fastest machine cycle supports $1T_{SYS}$ @ $F_{SYS} \leqslant 24MHz$
  - The fastest machine cycle supports $2T_{SYS}$ @ $F_{SYS} = 48MHz$
- **Memory**
  - Maximum program FLASH: 16K×8Bit
  - Maximum Data FLASH: 1K×8Bit
  - General RAM: 256×8Bit
  - Maximum universal XRAM: 1K×8Bit
  - Program FLASH supports partition protection
- **4 oscillation modes**
  - HSI-Internal RC oscillation: 48MHz
  - HSE-external crystal oscillation: 8MHz/16MHz
  - LSE-external crystal oscillation: 32.768KHz
  - LSI-Internal low-power oscillation: 125KHz
- **Low voltage reset function (LVR)**
  - 1.8V/2.0V/2.5V/3.5V
- **Low-voltage detection function (LVD)**
  - 2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V
- **GPIO**
  - Up to 22 GPIOs
  - All digital functions can be assigned to any GPIO
  - Both support up/down resistance function
  - Both support edge (rising edge/falling edge/double edge) interrupt
  - Support wake-up function
- **Interrupt source**
  - Support all external port interrupts
  - Up to 7 timer interrupts
  - Other peripheral interrupts
- **Timer**
  - WDT timer (watchdog timer)
  - Up to 5 timers:
  - Timer0/1, Timer2, Timer3/4
  - LSE Timer (support sleep wake function)
  - WUT (wake-up timer)
  - BRT (independent serial port baud rate clock generator)
- **Communication module**
  - 1x SPI (communication rate up to 6Mb/s)
  - 1x I2C (communication rate up to 400Kb/s)
  - Up to 2x UART (baud rate up to 1Mb/s)
- **Operating voltage range**
  - 2.1V-5.5V
- **Operating temperature range**
  - -40℃～105℃
- **Buzzer driver**
  - 50% duty cycle, frequency can be set freely
- **Enhanced EPWM**
  - Up to 6 channels enhanced PWM
  - Up to 6 mutually independent cycle counters
  - Support independent/complementary/synchronous/group mode
  - Support edge alignment/center alignment
  - Support complementary mode dead zone delay function
  - Support mask function and brake function
- **High-precision 12-bit ADC**
  - All GPIOs (22I/Os) support AD channels
  - Optional reference voltage (1.2V/2.0V/2.4V/3.0V/VDD)
  - Can detect internal 1.2V reference voltage
  - Support hardware trigger start conversion function
  - Support a set of result digital comparison function
- **Two analog comparators (ACMP0/1)**
  - 6 options for positive terminal, internal 1.2V/VDD voltage divider for negative terminal
  - Comparator supports unilateral/bilateral hysteresis
  - Hysteresis voltage optional 10/20/60mV
  - Support comparison output to trigger EPWM brake
  - The internal 1.2V/VDD divider of the negative terminal can be connected to the internal ADC channel
- **Two-way operational amplifier (OP0/1)**
  - Three terminals of each op amp are multiplexed with GPIO port
  - The positive end supports internal 1.2V input
  - Support two modes of op amp/comparator
  - Op amp output can be connected to internal ADC channel
  - The output of the op amp can be connected to the input of the internal analog comparator
  - Support offset voltage software trimming
- **Programmable gain amplifier (PGA)**
  - Support offset voltage software trimming
  - With sample and hold circuit (used with ADC)
  - Multi-stage gain optional (1/2/4/8/16/32/64/128 times)
  - Support single-ended/pseudo-differential input
  - PGA output can be connected to the internal ADC channel
  - PGA output can be connected to internal analog

- **Low power mode**
  - Idle mode (IDLE)
  - Sleep mode (STOP, Power consumption approx. 6uA)

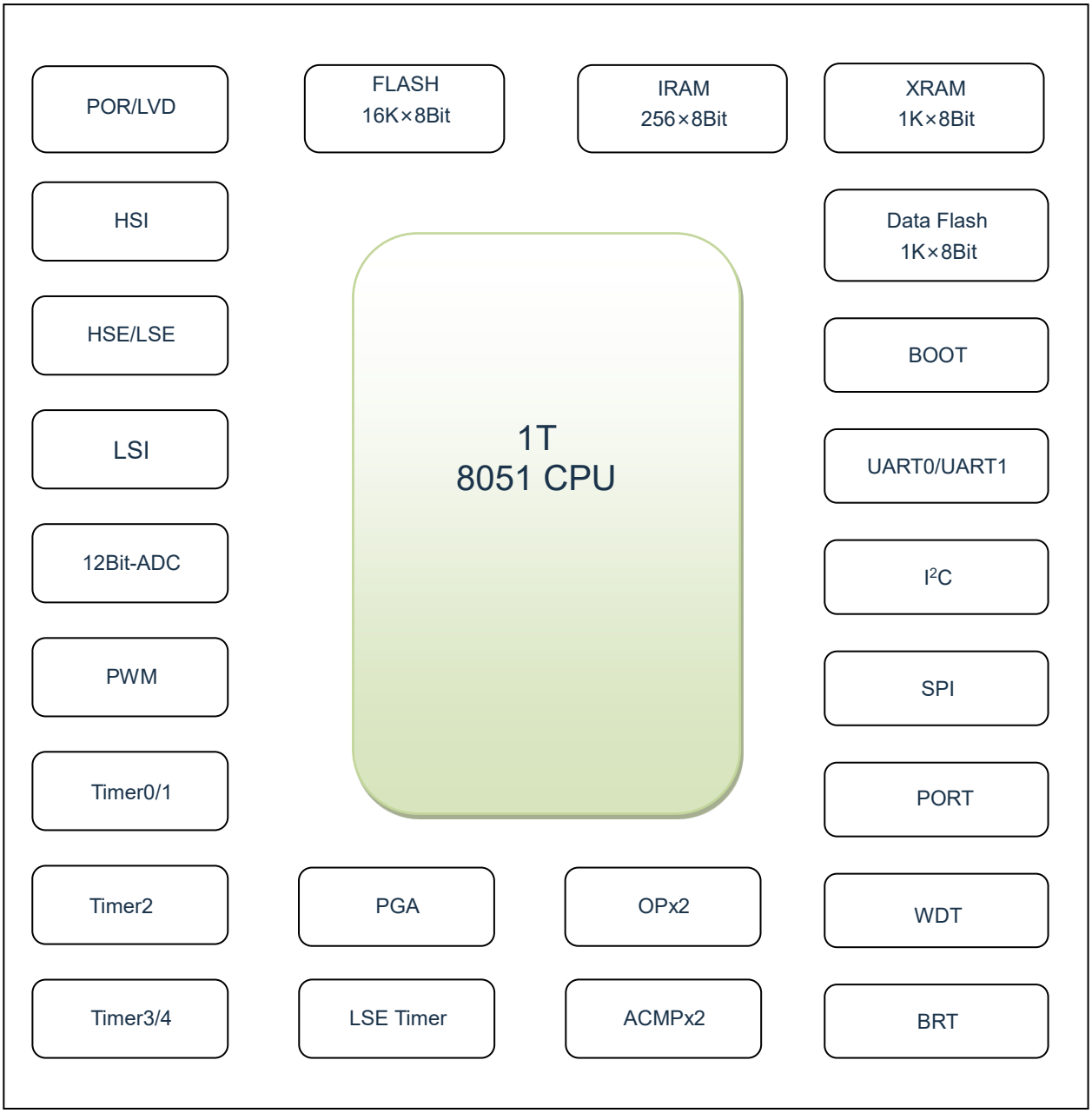
comparator input

- **Support 96-bit unique ID number (UID)**
  - Each chip has an independent ID number
- **Support two-wire serial programming and debugging**

Model description:

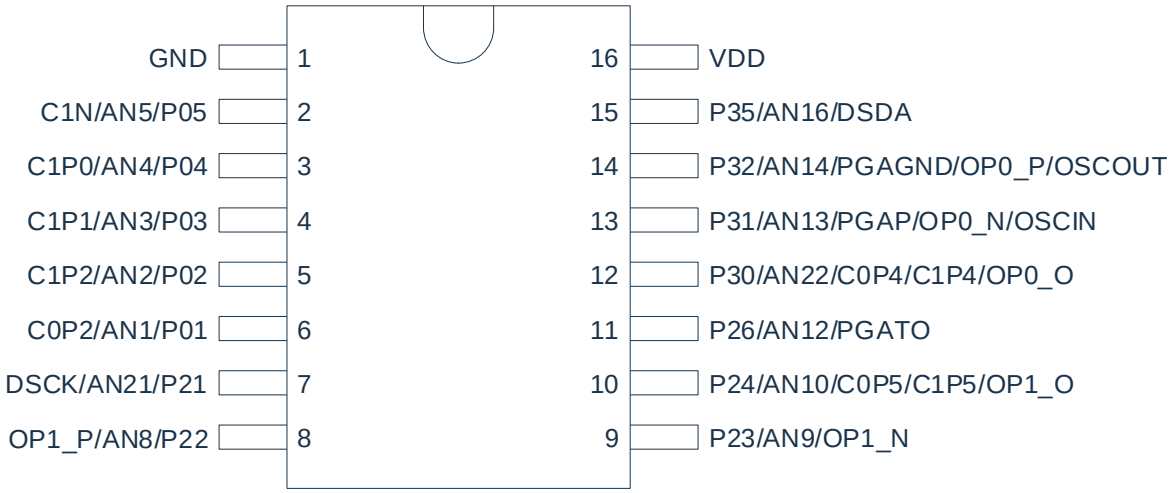
PRODUCT	FLASH	RAM	XRAM	DataFlash	I/O	ADC	ACMP	OPA	PGA	PACKAGE
CMS80F2313	16KB	256B	1KB	1KB	14	12Bit×14	2 channels	2 channels	1 channel	SOP16
CMS80F2316	16KB	256B	1KB	1KB	18	12Bit×18	2 channels	2 channels	1 channel	SOP20
CMS80F2317	16KB	256B	1KB	1KB	22	12Bit×22	2 channels	2 channels	1 channel	SOP24

1.2 System Block Diagram



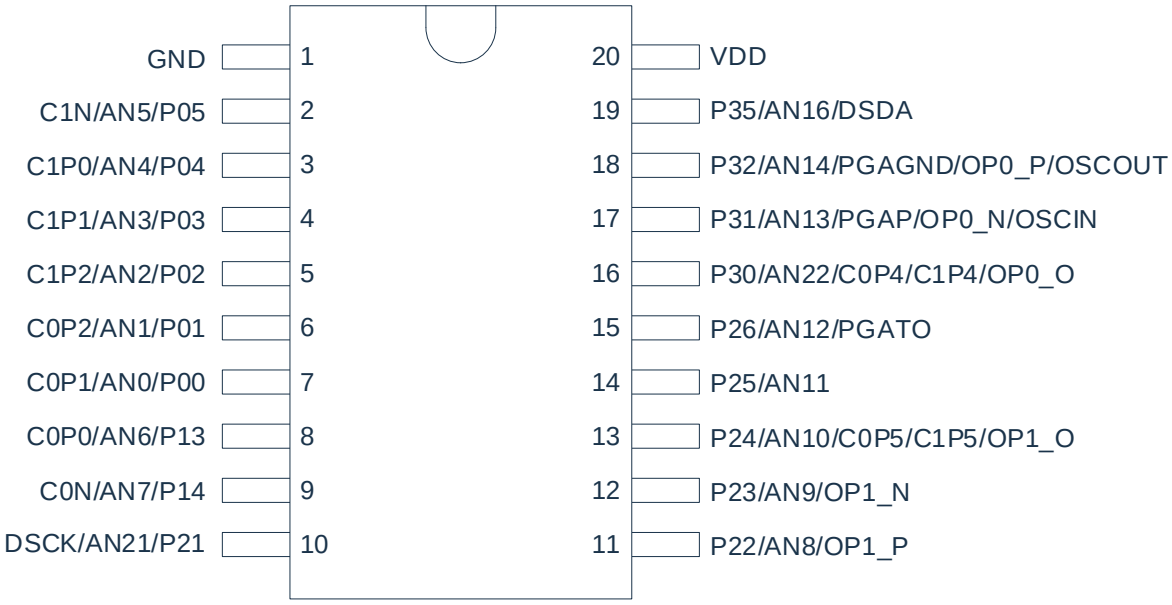
1.3 Pin Distribution

1.3.1 CMS80F2313



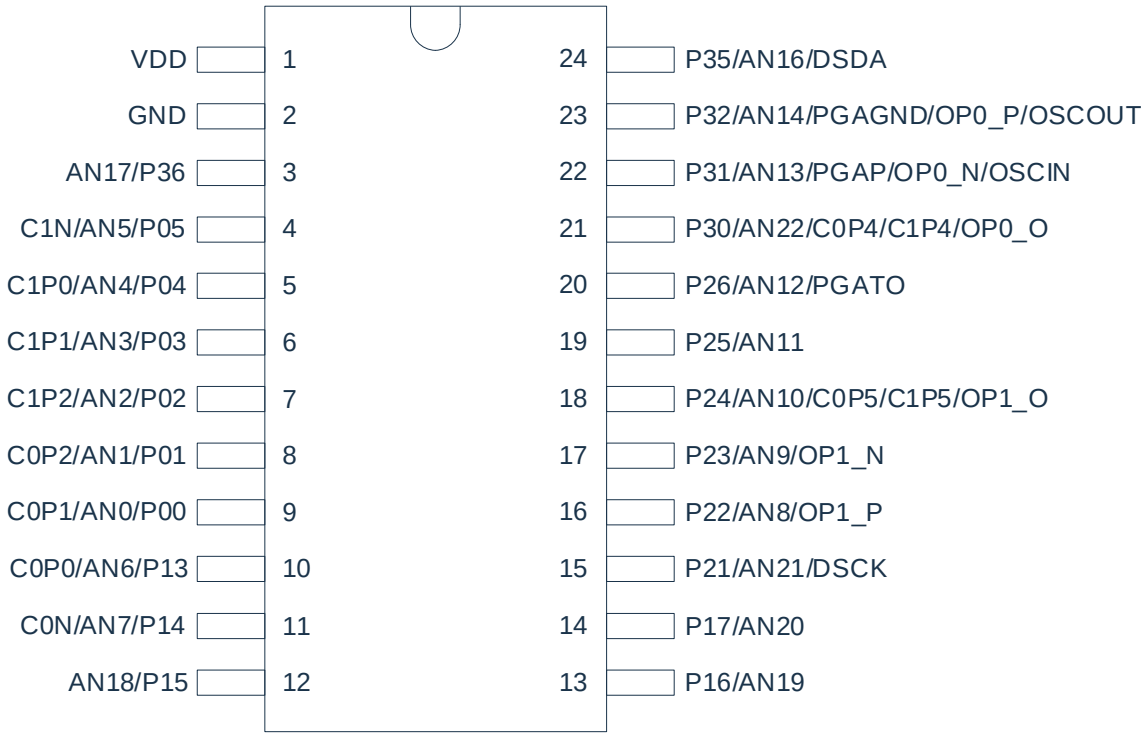
CMS80F2313

1.3.2 CMS80F2316



CMS80F2316

1.3.3 CMS80F2317



CMS80F2317

Pin Description:

Pin Name	Function	I/O	Description
P00/AN0/C0P1	P00	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN0	I	ADC channel 0 input
	C0P1	I	Comparator 0 positive channel 1 input
P01/AN1/C0P2	P01	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN1	I	ADC channel 1 input
	C0P2	I	Comparator 0 positive channel 2 input
P02/AN2/C1P2	P02	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN2	I	ADC channel 2 input
	C1P2	I	Comparator 1 positive channel 2 input
P03/AN3/C1P1	P03	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN3	I	ADC channel 3 input
	C1P1	I	Comparator 1 positive channel 1 input
P04/AN4/C1P0	P04	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN4	I	ADC channel 4 input
	C1P0	I	Comparator 1 positive channel 0 input
P05/AN5/C1N	P05	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN5	I	ADC channel 5 input
	C1N	I	Comparator 1 negative channel input
P13/AN6/C0P0	P13	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN6	I	ADC channel 6 input

Pin Name	Function	I/O	Description
	C0P0	I	Comparator 0 positive channel 0 input
P14/AN7/C0N	P14	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN7	I	ADC channel 7 input
	C0N	I	Comparator 0 negative channel input
P15/AN18	P15	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN18	I	ADC channel 18 input
P16/AN19	P16	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN19	I	ADC channel 19 input
P17/AN20	P17	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN20	I	ADC channel 20 input
P21/AN21/DSCK	P21	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN21	I	ADC channel 21 input
	DSCK	I/O	Programming, debugging clock inputs and outputs
P22/AN8/OP1_P	P22	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN8	I	ADC channel 8 input
	OP1_P	I	Op-amp 1 positive input
P23/AN9/OP1_N	P23	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN9	I	ADC channel 9 input
	OP1_N	I	Op-amp 1 negative input
P24/AN10/C0P5/C1P5/OP1_O	P24	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN10	I	ADC channel 10 input
	C0P5	I	Comparator 0 positive side channel 5 input
	C1P5	I	Comparator 1 positive channel 5 input
	OP1_O	O	Op-amp 1 output
P25/AN11	P25	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN11	I	ADC channel 11 input
P26/AN12/PGATO	P26	I/O	GPIO, configure input and output through registers, pull-up and pull-down functions
	AN12	I	ADC channel 12 input
	PGATO	O	PGA test output
P30/AN22/C0P4/C1P4/OP0_O	P30	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN22	I	ADC channel 22 input
	C0P4	I	Comparator 0 positive side channel 4 input
	C1P4	I	Comparator 1 positive channel 4 input
	OP0_O	O	Op-amp 0 output
P31/AN13/OSCIN/OP0_N/PGAP	P31	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN13	I	ADC channel 13 input
	OSCIN	I	External oscillation input
	OP0_N	I	Op-amp 0 negative input
	PGAP	I	PGA positive input
P32/AN14/OSCOUT/OP0_P/PGAGND	P32	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN14	I	ADC channel 14 input

Pin Name	Function	I/O	Description
	OSCOUT	O	External oscillation output
	OP0_P	I	Op-amp 0 positive input
	PGAGND	I	PGA feedback ground input
P35/AN16/DSDA	P35	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN16	I	ADC channel 16 input
	DSDA	I/O	Programming and debugging data input and output
P36/AN17	P36	I/O	GPIO configuration of input and output, pull-up and pull-down through registers
	AN17	I	ADC channel 17 input
VDD		P	Power supply voltage input pin
VSS		P	Ground pin

1.4 System Configuration Register

The system configuration register (CONFIG) is the FLASH option for the MCU initial condition. It can only be programmed by the CMS writer and cannot be accessed and operated by the user. It contains the following:

1. WDT (watchdog operating mode selection)
   - ENABLE — Forced to enable WDT
   - SOFTWARE CONTROL (DEFAULT) — WDT operating mode is controlled by the WDTRE bit in the WDCON register.
2. PROTECT
   - ENABLE — The Flash code is encrypted and read as 00H. And it is forbidden to enter debug mode
   - DISABLE (DEFAULT) — The Flash code is not encrypted
3. FLASH_DATA_PROTECT
   - DISABLE — The FLASH data area is not encrypted
   - ENABLE (DEFAULT) — The Flash data area is encrypted, the value read by the emulator after encryption is 00H
4. LVR (low voltage reset)
   - 1.8V (DEFAULT)
   - 2.0V
   - 2.5V
   - 3.5V
5. DEBUG (debug mode)
   - DISABLE (DEFAULT) — Debug mode is forbidden, P21 and P35 are used as ordinary IO ports
   - ENABLE — Debug mode is enabled, P21 and P35 are configured as debug ports (DSCK,DSDA), and other functions corresponding to the pins are turned off.
6. OSC (oscillation mode)
   - HSI (DEFAULT) — 48MHz
   - HSE — OSCIN and OSCOUT are configured as oscillation ports
   - LSE(32.768KHz) — OSCIN and OSCOUT are configured as oscillation ports
   - LSI(125KHz) — 125KHz
7. OSC_PRESCALE (oscillation output prescaler selection)
   - F_{OSC}/1 (DEFAULT) — (System clock selects HSI and HSI_FS=F_{HSI}/1 then F_{CPU}=F_{HSI}/2)
   - F_{OSC}/2
   - F_{OSC}/4
   - F_{OSC}/8
8. HSI_FS (internal RC oscillator frequency selection)
   - F_{HSI}/1 — 48MHz
   - F_{HSI}/2 — 24MHz
   - F_{HSI}/3 — 16MHz
   - F_{HSI}/6 (DEFAULT) — 8MHz
9. EXT_RESET (external reset configuration)
   - DISABLE (DEFAULT) — External reset disabled
   - ENABLE — External reset enable
   - ENABLE(OPEN PULLUP) — External reset enable and open internal pull-up resistor at the reset port

10. EXT_RESETSEL (external reset port selection)

- P00
- P01
- P02
- P03
- P04
- P05
- P13
- P14
- P15
- P16
- P17
- P21
- P22
- P23
- P24
- P25
- P26
- P30
- P31
- P32
- P35
- P36

11. WAKE UP_WAIT TIME (the default waiting time of wake up after sleep mode is 1.0s)

- 50us
- 100us
- 500us
- 1ms
- 5ms
- 10ms
- 500ms
- 1.0s (default)

12. CPU_WAITCLOCK (memory wait clock selection)

- 1*System Clock (1T) (default)
- 2*System Clock (2T)
- 3*System Clock (3T)
- 4*System Clock (4T)
- 5*System Clock (5T)
- 6*System Clock (6T)
- 7*System Clock (7T)
- 8*System Clock (8T)

13. WRITE_PROTECT program partition protection (intervals can be protected, all default intervals are unprotected)

- 0-2K (0000H-07FFH protected/unprotected)
- 2-4K (0800H-0FFFH protected/unprotected)
- 4-6K (1000H-17FFH protected/unprotected)
- 6-8K (1800H-1FFFH protected/unprotected)
- 8-10K (2000H-27FFH protected/unprotected)
- 10-12K (2800H-2FFFH protected/unprotected)
- 12-14K (3000H-37FFH protected/unprotected)
- 14-16K (3800H-3FFFH protected/unprotected)

14. BOOT space selection

- BOOT_DIS (default) BOOT area prohibition
- BOOT_1K BOOT area space is 1K
- BOOT_2K BOOT area space is 2K
- BOOT_4K BOOT area space is 4K

1.5 Online Serial Programming

The microcontroller can be serially programmed in the final application circuit. Programming can be simply done by the following four lines:

- Power line
- Ground line
- Data line
- Clock line

This allows the user to fabricate circuit boards using unprogrammed devices and just to program the microcontroller before the product is delivered. Thereby the latest version of firmware or custom firmware can be programmed into the microcontroller.

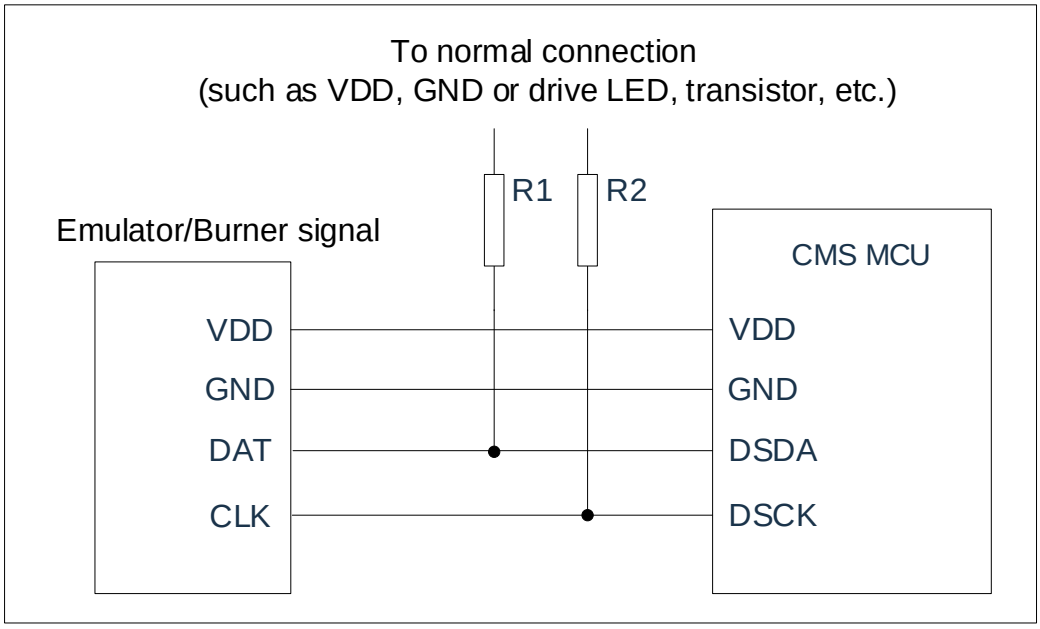


Figure 1-1: Typical online serial programming connection method

In the above figure, R1 and R2 are electrically isolated devices, often replaced by resistors with the following resistance values: R1≥4.7K, R2≥4.7K.

Note that the DSDA prohibits the connection of pull-down resistors during programming and debugging. If the actual circuit needs to connect a pull-down resistor, it is recommended to use a jumper structure to disconnect the pull-down resistor during programming/debugging and then connect the pull-down resistor after completion.

1.6 Online Debugging Mode

The chip supports 2-wire (DSCK, DSDA) online debugging function. If you use the online debugging function, you need to set DEBUG in the system configuration register to ENABLE. When using debug mode, you need to pay attention to the following points:

- In debugging state, the DSCK and DSDA ports are dedicated debugging ports, and their GPIO and multiplexing functions cannot be realized.
- When entering the sleep mode/idle mode (STOP/IDLE) in the debug state, the system power supply and oscillator will not stop working, and the sleep wake-up function can be simulated in this state. If you need to pay attention to power consumption, it is recommended to turn off the debugging function before testing the actual sleep current of the chip.
- Pause in the debug state, other functional peripherals continue to run, WDT, Timer0/1/2/3/4 counters will stop. But if Timer1/4 is used as the baud rate generator of UART0/1/2/3, Timer1/4 will continue to run in the pause state. Peripherals that continue to run in the paused state may generate interrupts, so be careful when debugging.

2. CENTRAL PROCESSING UNIT (CPU)

2.1 Memory

2.1.1 Program Memory

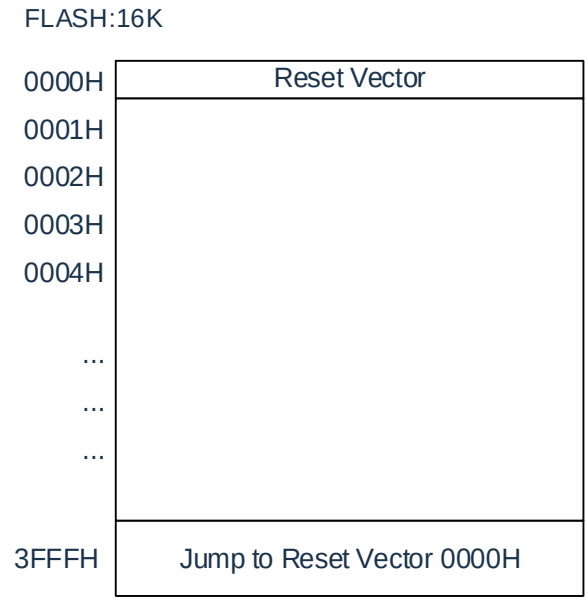


Figure 2-1: Program memory space

A 16-bit program counter can reach up to addresses of 64K bytes, But this chip can only store16K bytes.

The above figure shows the lower area of the program memory. After reset, the CPU starts at 0000H. Each interrupt is assigned to a fixed address interrupt in the program memory, which leads the CPU jumps to the address to start excuting the service program, such as external interrupt 1, the assigned address of which is 000BH. If using external interrupt 1, its service program must start from the address of 0013H. If the interrupt is not used, its service address is used as a normal program storage address.

2.1.1.1 BOOT Partition

The program area space size is 16K*8Bit, in which the program area is divided into BOOT area and APROM area, the size of BOOT area is allocated by the system configuration register, see Chapter 1.4. The space address allocation of BOOT area and APROM area is shown in Table 2.1 below.

Table 2.1 Program memory area space address allocation

16K (program memory area 0000H-3FFFFH)				
Address space allocation method	APROM Area		BOOT Area	
Mode 0	16K	0000H-3FFFH	--	--
Mode 1	15K	0000H-3BFFH	1K	3C00H-3FFFH
Mode 2	14K	0000H-37FFH	2K	3800H-3FFFH
Mode 3	12K	0000H-2FFFH	4K	3000H-3FFFH

When the chip is powered on, if the program is started from BOOT area, it needs to meet: the address space allocation method is 1/2/3 (set BOOT_1K/BOOT_2K/BOOT_4K by CONFIG), otherwise the program will be started from APROM area.

Take the 1K space in BOOT area as an example: CONFIG configures BOOT_1K, after the chip is powered on, the program starts from address 3C00. If the program needs to switch between the BOOT area and APROM area, you need to write 0xAA/0x55 to BOOTCON (see register description), and then perform a software reset or generate a watchdog reset.

When power-on reset, external reset or voltage reset, BOOTCON reset value is 0x00, software reset and watchdog reset cannot clear this register.

BOOT Control Register (BOOTCON)

F691H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BOOTCON	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7-Bit0	D7-D0	BOOT area control bit (this register can only be written when the chip is configured as BOOT_1K/BOOT_2K/BOOT_4K)
	0x55=	If you switch from APROM area to BOOT area, you need to write 0x55 to it, then execute software reset or generate watchdog reset
	0xAA=	If you switch from BOOT area to APROM area, you need to write 0xAA to it, then execute software reset or generate watchdog reset
	Others =	Invalid

For example, after the chip is powered on and booted from the BOOT area, it is switched to the APROM area using a software reset with the following configuration:

1) BOOT_ID register needs to be written AAH

```
MOV   DPTR, #BOOT_ID
MOV   A,#0AAH
MOVX@DPTR,A
```

2) Perform a software reset

```
MOV   TA, #0AAH
```

```
MOV   TA, #055H
MOV   WDCON, #080H
```

For example, using the software reset method, and then switching from the APROM area to the BOOT area, the configuration is as follows.

1) BOOT_ID register needs to be written 55H

```
MOV   DPTR, #BOOT_ID
MOV   A,#055H
MOVX@DPTR,A
```

2) Perform a software reset

```
MOV   TA, #0AAH
MOV   TA, #055H
MOV   WDCON, #080H
```

Note: When the BOOT function is active, the program in the APROM needs to ensure that the PC does not overflow (overflow means that the PC is outside the address range of the APROM), and if there is a PC overflow, the system may run abnormally.

2.1.2 Reset Vector (0000H)

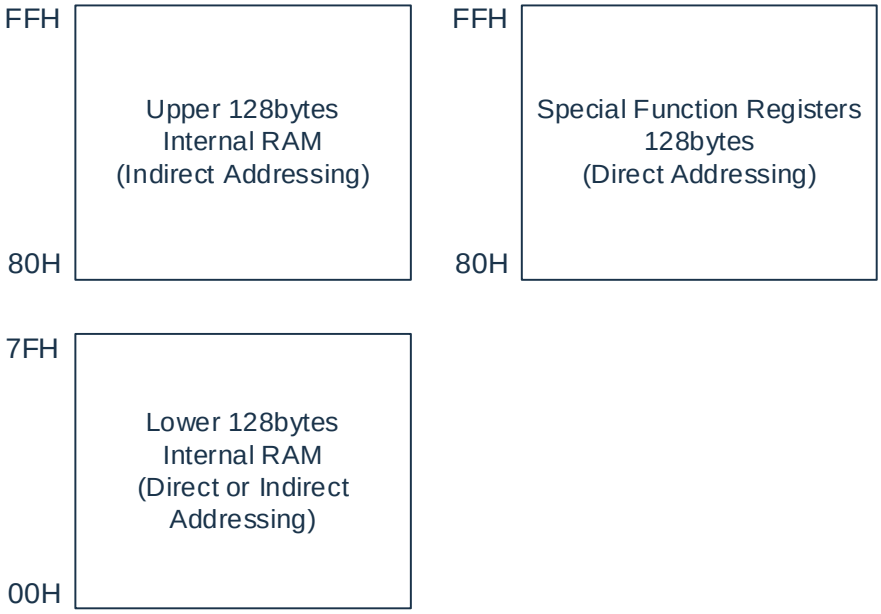
Single chip microcomputer posses a system reset vector with a word length (0000H).

After the reset occurs, the program will start again from 0000H, and the system registers will be recover to the default values. The following program demonstrates show to define the reset vector in FLASH.

Example: Define reset vector

```
        ORG     0000H       ;System reset vector
        LJMP    START
        ORG     0010H       ;User Program Initiation
START:
        ...                 ;User Program
        ...
        END                 ;End of proceedings
```

2.1.3 Data Memory (IRAM)



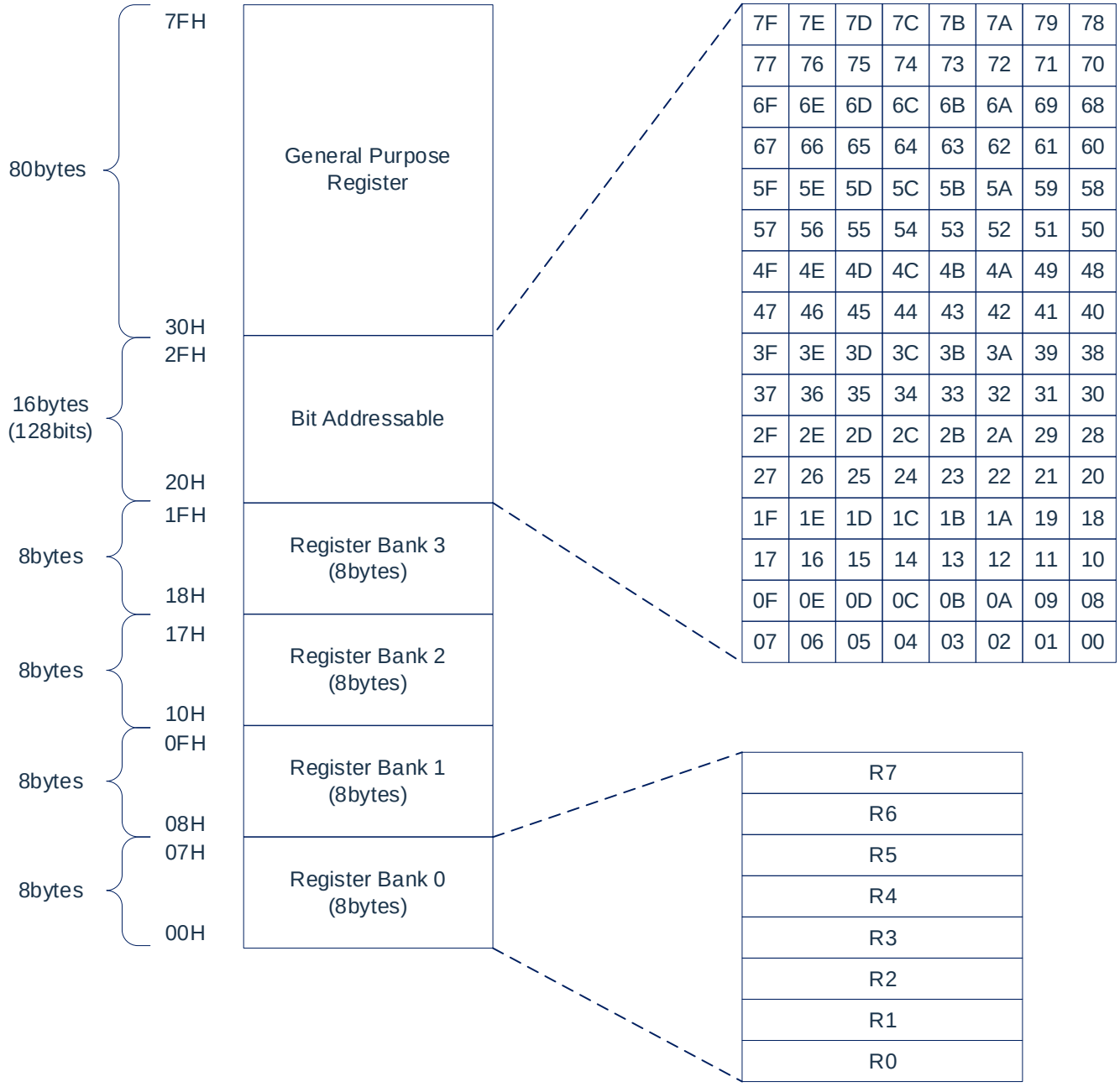
Internal data register is divided into 3 parts: low 128 bytes, high 128 bytes, SFR.

The internal data register address is one byte wide, which means that the address space is only 256 bytes wide. However, in fact 384 bytes wide is available if adjusting using internal RAM addressing method. Direct and indirect addressing memory space that are higher than 7FH enter different memory space, the diagram above indicates high 128 bytes and SFR occupy the same area which is 80H to FFH, but they themselves are independent.

The diagram above shows the low 128 bytes RAM for all 8051 series. The lowest 32 bytes compose 4 registers, and the program instructions can call registers from R0 to R7, two bits in the program state determine which register group to use. It is more efficient to use code space in this way, because register instruction is shorter than direct addressing instruction.

The 16 bytes after the register group compose a bit-addressable memory space. 8051 instruction setting includes bit instruction width operations, but the 128 bits in this area can be directly addressed through these instructions. The address of the area is from 20H to 2FH.

All bytes from low 128 bytes in general register can be accessed directly or indirectly, and high 128 bytes can only be accessed indirectly. These areas are used as data RAM and stack.



2.1.4 Special Function Register Table (SFR)

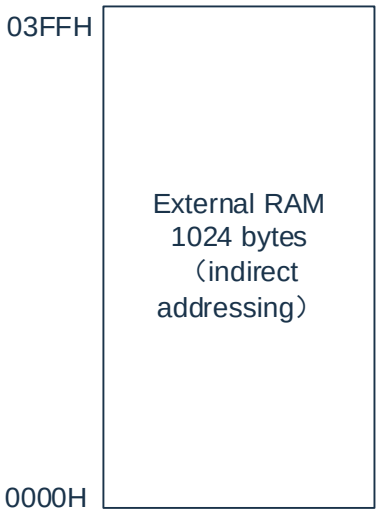
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	--	--	--	MLOCK	MADRL	MADRH	MDATA	MCTRL
0xF0	B	I2CSADR	I2CSCR	I2CSBUF	I2CMSA	I2CMCR	I2CMBUF	I2CMTP
0xE8	--	ADCON2	SCON1	SBUF1	SPCR	SPSR	SPDR	SSCR
0xE0	ACC	--	TL4	TH4	--	--	--	--
0xD8	--	--	TL3	TH3	ADRESL	ADRESH	ADCON1	ADCON0
0xD0	PSW	ADCMPC	T34MOD	ADDLYL	ADCMPL	ADCMPH	--	--
0xC8	T2CON	T2IF	RLDL	RLDH	TL2	TH2	CCEN	T2IE
0xC0	--	--	CCL1	CCH1	CCL2	CCH2	CCL3	CCH3
0xB8	IP	EIP1	EIP2	--	WUTCRL	WUTCRH	BUZDIV	BUZCON
0xB0	P3	--	EIF2	--	P0EXTIF	P1EXTIF	P2EXTIF	P3EXTIF
0xA8	IE	--	EIE2	--	P0EXTIE	P1EXTIE	P2EXTIE	P3EXTIE
0xA0	P2	P1TRIS	P2TRIS	P3TRIS	--	--	--	--
0x98	SCON0	SBUF	P0TRIS	--	--	--	--	--
0x90	P1	FUNCCR	--	--	--	--	TA	WDCON
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	CLKDIV
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Note: The lower four digits of the SFR address are 0000 or 1000 and can be addressed, such as P0, TCON and P1.

Addresses marked with "--" in the table are not allowed to be accessed.

2.1.5 External Data Memory (XRAM)

There is 1K bytes XRAM inside the chip, this area has no connection with RAM/FLASH and can be read and written through an 8-bit SFR.



XRAM/XSFR operation:

DPTR includes two sets of pointers through the DPTR data pointer operation: DPTR0, DPTR1.

Each set of pointers includes two 8-bit registers: DPTR0= {DPH0, DPL0}; DPTR1= {DPH1, DPL1};

The assembly code is as follows:

```
MOV     DPTR,#0001H
MOV     A,#5AH
MOVX    @DPTR,A      ; Write the data in A to the XRAM address 0001H
```

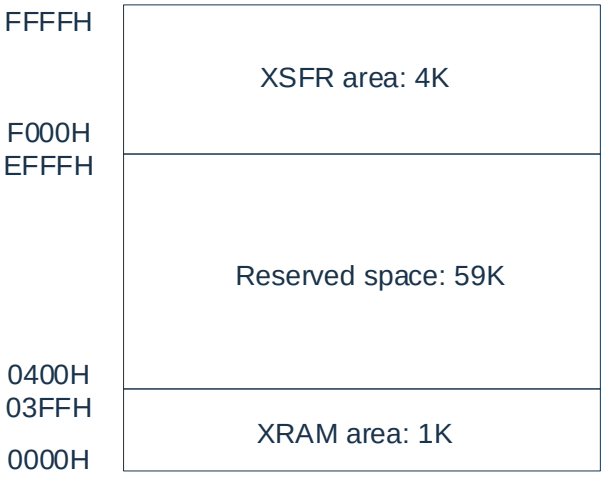
Through the MOVX indirect addressing operation, the assembly code is as follows:

```
MOV     R0,#01H
MOV     A,#5AH
MOVX    @R0,A        ; Write the data in A to XRAM address 01H, the upper 8 bits are
                     determined by DPH0/1
```

When Target-->Memory Model is set to Large in Keil51, the C compiler will use XRAM as the variable address. Generally use the DPTR performs XRAM/XSFR operations.

2.1.6 Special Function Register Table (XSFR)

XSFR is a special register sharing the address space with XRAM. It mainly includes: port control register and other function control registers. Its addressing range is as follows:



XSFR list:

Address	Symbol	Description
F000H	P00CFG	P0.0 port configuration register
F001H	P01CFG	P0.1 port configuration register
F002H	P02CFG	P0.2 port configuration register
F003H	P03CFG	P0.3 port configuration register
F004H	P04CFG	P0.4 port configuration register
F005H	P05CFG	P0.5 port configuration register
F006H	--	--
F007H	--	--
F009H	P0OD	P0 port open-drain control register
F00AH	P0UP	P0 port pull-up resistor control register
F00BH	P0RD	P0 port pull-down resistor control register
F00CH	P0DR	P0 port drive current control register
F00DH	P0SR	P0 port slope control register
F00EH	P0DS	P0 port data input selection register
--	--	--
F013H	P13CFG	P1.3 port configuration register
F014H	P14CFG	P1.4 port configuration register
F015H	P15CFG	P1.5 port configuration register
F016H	P16CFG	P1.6 port configuration register
F017H	P17CFG	P1.7 port configuration register
F019H	P1OD	P1 port open-drain control register
F01AH	P1UP	P1 port pull-up resistor control register
F01BH	P1RD	P1 port pull-down resistor control register
F01CH	P1DR	P1 port drive current control register
F01DH	P1SR	P1 port slope control register
F01EH	P1DS	P1 port data input selection register
--	--	--
F020H	--	--

Address	Symbol	Description
F021H	P21CFG	P2.1 port configuration register
F022H	P22CFG	P2.2 port configuration register
F023H	P23CFG	P2.3 port configuration register
F024H	P24CFG	P2.4 port configuration register
F025H	P25CFG	P2.5 port configuration register
F026H	P26CFG	P2.6 port configuration register
F027H	--	--
F029H	P2OD	P2 port open-drain control register
F02AH	P2UP	P2 port pull-up resistor control register
F02BH	P2RD	P2 port pull-down resistor control register
F02CH	P2DR	P2 port drive current control register
F02DH	P2SR	P2 port slope control register
F02EH	P2DS	P2 port data input selection register
--	--	--
F030H	P30CFG	P3.0 port configuration register
F031H	P31CFG	P3.1 port configuration register
F032H	P32CFG	P3.2 port configuration register
F033H	--	--
F034H	--	--
F035H	P35CFG	P3.5 port configuration register
F036H	P36CFG	P3.6 port configuration register
F037H	--	--
F039H	P3OD	P3 port open-drain control register
F03AH	P3UP	P3 port pull-up resistor control register
F03BH	P3RD	P3 port pull-down resistor control register
F03CH	P3DR	P3 port drive current control register
F03DH	P3SR	P3 port slope control register
F03EH	P3DS	P3 port data input selection register
--	--	--
F080H	P00EICFG	P0.0 port interrupt control register
F081H	P01EICFG	P0.1 port interrupt control register
F082H	P02EICFG	P0.2 port interrupt control register
F083H	P03EICFG	P0.3 port interrupt control register
F084H	P04EICFG	P0.4 port interrupt control register
F085H	P05EICFG	P0.5 port interrupt control register
--	--	--
F08BH	P13EICFG	P1.3 port interrupt control register
F08CH	P14EICFG	P1.4 port interrupt control register
F08DH	P15EICFG	P1.5 port interrupt control register
F08EH	P16EICFG	P1.6 port interrupt control register
F08FH	P17EICFG	P1.7 port interrupt control register
F090H	--	--
F091H	P21EICFG	P2.1 port interrupt control register
F092H	P22EICFG	P2.2 port interrupt control register
F093H	P23EICFG	P2.3 port interrupt control register
F094H	P24EICFG	P2.4 port interrupt control register
F095H	P25EICFG	P2.5 port interrupt control register

Address	Symbol	Description
F096H	P26EICFG	P2.6 port interrupt control register
F097H	--	--
F098H	P30EICFG	P3.0 port interrupt control register
F099H	P31EICFG	P3.1 port interrupt control register
F09AH	P32EICFG	P3.2 port interrupt control register
F09BH	--	--
F09CH	--	--
F09DH	P35EICFG	P3.5 port interrupt control register
F09EH	P36EICFG	P3.6 port interrupt control register
F09FH	--	--
--	--	--
F0C0H	PS_INT0	External interrupt 0 input port configure register
F0C1H	PS_INT1	External interrupt 1 input port configure register
F0C2H	PS_T0	Timer0 external clock input port configure register
F0C3H	PS_T0G	Timer0 gate control input port configure register
F0C4H	PS_T1	Timer1 external clock input port configure register
F0C5H	PS_T1G	Timer1 gate control input port configure register
F0C6H	PS_T2	Timer2 external event or gate control input port configure register
F0C7H	PS_T2EX	Timer2 falling edge auto-reload input port configure register
F0C8H	PS_CAP0	Timer2 input capture channel 0 port configure register
F0C9H	PS_CAP1	Timer2 input capture channel 1 port configure register
F0CAH	PS_CAP2	Timer2 input capture channel 2 port configure register
F0CBH	PS_CAP3	Timer2 input capture channel 3 port configure register
F0CCH	PS_ADET	ADC external trigger input port configure register
F0CDH	PS_FB	PWM external brake signal port configure register
--	--	--
F120H	PWMCON	PWM control register
F121H	PWMOE	PWM output enable register
F122H	PWMPINV	PWM output polarity selection register
F123H	PWM01PSC	PWM0/PWM1 prescaler control register
F124H	PWM23PSC	PWM2/PWM3 prescaler control register
F125H	PWM45PSC	PWM4/PWM5 prescaler control register
F126H	PWMCNTE	PWM count start control register
F127H	PWMCNTM	PWM count mode selection register
F128H	PWMCNTCLR	PWM counter clear control register
F129H	PWMLOADEN	PWM load enable control register
F12AH	PWM0DIV	PWM0 frequency division control register
F12BH	PWM1DIV	PWM1 frequency division control register
F12CH	PWM2DIV	PWM2 frequency division control register
F12DH	PWM3DIV	PWM3 frequency division control register
F12EH	PWM4DIV	PWM4 frequency division control register
F12FH	PWM5DIV	PWM5 frequency division control register
F130H	PWMP0L	PWM0 periodic data register lower 8 bits
F131H	PWMP0H	PWM0 periodic data register higher 8 bits
F132H	PWMP1L	PWM1 periodic data register lower 8 bits
F133H	PWMP1H	PWM1 periodic data register higher 8 bits

Address	Symbol	Description
F134H	PWMP2L	PWM2 periodic data register lower 8 bits
F135H	PWMP2H	PWM2 periodic data register higher 8 bits
F136H	PWMP3L	PWM3 periodic data register lower 8 bits
F137H	PWMP3H	PWM3 periodic data register higher 8 bits
F138H	PWMP4L	PWM4 periodic data register lower 8 bits
F139H	PWMP4H	PWM4 periodic data register higher 8 bits
F13AH	PWMP5L	PWM5 periodic data register lower 8 bits
F13BH	PWMP5H	PWM5 periodic data register higher 8 bits
--	--	--
F140H	PWMD0L	PWM0 compare data register lower 8 bits
F141H	PWMD0H	PWM0 compare data register higher 8 bits
F142H	PWMD1L	PWM1 compare data register lower 8 bits
F143H	PWMD1H	PWM1 compare data register higher 8 bits
F144H	PWMD2L	PWM2 compare data register lower 8 bits
F145H	PWMD2H	PWM2 compare data register higher 8 bits
F146H	PWMD3L	PWM3 compare data register lower 8 bits
F147H	PWMD3H	PWM3 compare data register higher 8 bits
F148H	PWMD4L	PWM4 compare data register lower 8 bits
F149H	PWMD4H	PWM4 compare data register higher 8 bits
F14AH	PWMD5L	PWM5 compare data register lower 8 bits
F14BH	PWMD5H	PWM5 compare data register higher 8 bits
--	--	--
F150H	PWMDD0L	PWM0 asymmetric downward comparison data register lower 8 bits
F151H	PWMDD0H	PWM0 asymmetric downward comparison data register high 8 bits
F152H	PWMDD1L	PWM1 asymmetric downward comparison data register lower 8 bits
F153H	PWMDD1H	PWM1 asymmetric downward comparison data register high 8 bits
F154H	PWMDD2L	PWM2 asymmetric downward comparison data register lower 8 bits
F155H	PWMDD2H	PWM2 asymmetric downward comparison data register high 8 bits
F156H	PWMDD3L	PWM3 asymmetric downward comparison data register lower 8 bits
F157H	PWMDD3H	PWM3 asymmetric downward comparison data register high 8 bits
F158H	PWMDD4L	PWM4 asymmetric downward comparison data register lower 8 bits
F159H	PWMDD4H	PWM4 asymmetric downward comparison data register high 8 bits
F15AH	PWMDD5L	PWM5 asymmetric downward comparison data register lower 8 bits
F15BH	PWMDD5H	PWM5 asymmetric downward comparison data register high 8 bits
--	--	--
F160H	PWMDTE	PWM programmable dead time delay control register
F161H	PWM01DT	PWM0/PWM1 programmable dead time delay register
F162H	PWM23DT	PWM2/PWM3 programmable dead time delay register
F163H	PWM45DT	PWM4/PWM5 programmable dead time delay register r
F164H	PWMMASKE	PWM mask enable control register
F165H	PWMMASKD	PWM mask data register
F166H	PWMFBKC	PWM brake control register

Address	Symbol	Description
F167H	PWMFBKD	PWM brake data register
F168H	PWMPIE	PWM periodic interrupt enable register
F169H	PWMZIE	PWM zero interrupt enable register
F16AH	PWMUIE	PWM up compare interrupt enable register
F16BH	PWMDIE	PWM down compare interrupt enable register
F16CH	PWMPIF	PWM periodic interrupt flag register
F16DH	PWMZIF	PWM zero interrupt flag register
F16EH	PWMUIF	PWM up compare interrupt flag register
F16FH	PWMDIF	PWM down compare interrupt flag register
--	--	--
F500H	C0CON0	Comparator 0 control register 0
F501H	C0CON1	Comparator 0 control register 1
F502H	C0CON2	Comparator 0 control register 2
F503H	C1CON0	Comparator 1 control register 0
F504H	C1CON1	Comparator 1 control register 1
F505H	C1CON2	Comparator 1 control register 2
F506H	CNVRCON	Comparator reference voltage control register
F507H	CNFBCON	Comparator brake control register
F508H	CNIE	Comparator interrupt enable register
F509H	CNIF	Comparator interrupt flag register
F50AH	C0ADJE	Comparator 0 adjustment bit selection register
F50BH	C1ADJE	Comparator 1 adjustment bit selection register
F50CH	C0HYS	Comparator 0 hysteresis control register
F50DH	C1HYS	Comparator 1 hysteresis control register
--	--	--
F520H	OP0CON0	Op-amp 0 control register 0
F521H	OP0CON1	Op-amp 0 control register 1
F522H	--	--
F523H	OP1CON0	Op-amp 1 control register 0
F524H	OP1CON1	Op-amp 1 control register 1
F525H	--	Not used
F526H	OP0ADJE	Op-amp 0 adjustment bit selection register
F527H	OP1ADJE	Op-amp 1 adjustment bit selection register
--	--	--
F529H	PGACON0	PGA control register 0
F52AH	PGACON1	PGA control register 1
F52BH	PGACON2	PGA control register 2
F52CH	PGACON3	PGA control register 3
F52DH	PGAADJE	PGA adjustment bit selection register
--	--	Not used
F5C0H	BRTCON	BRT module control register
F5C1H	BRTDL	BRT timer load value lower 8 bits
F5C2H	BRTDH	BRT timer load value higher 8 bits
--	--	--
F690H	LVDCON	Power monitoring register
F691H	BOOTCON	BOOT control register
F692H	ADCLDO	ADC reference voltage control register

Address	Symbol	Description
--	--	-
F694H	LSECRL	LSE timer data register lower 8 bits
F695H	LSECRH	LSE timer data register higher 8 bits
F696H	LSECON	LSE timer control register
--	--	--
F5E0H	UID0	UID<7:0>
F5E1H	UID1	UID<15:8>
F5E2H	UID2	UID<23:16>
F5E3H	UID3	UID<31:24>
F5E4H	UID4	UID<39:32>
F5E5H	UID5	UID<47:40>
F5E6H	UID6	UID<55:48>
F5E7H	UID7	UID<63:56>
F5E8H	UID8	UID<71:64>
F5E9H	UID9	UID<79:72>
F5EAH	UID10	UID<87:80>
F5EBH	UID11	UID<95:88>

Note: Access to addresses marked with "--" in the table is Disabled.

2.2 Accumulator (ACC)

ALU is an 8-bit wide arithmetic logic unit, all the mathematical and logical operations of MCU are accomplished through it. It can carry out logical operations such as addition, subtraction and shift on data; ALU also controls the status bit (PSW status register), to indicate the state of the operation result.

ACC is an 8-bit register, the operation results of ALU could be stored in ACC.

2.3 B Register (B)

B Register is used when multiply and division instructions are used or it can be used as a general register when not using multiply and division instructions.

2.4 Stack Pointer Register (SP)

SP Register points to the address of the stack, after a reset, it goes to its initial values 0x07, it means that the stack area starts with the 08H of the IRAM address. The value of the SP can be modified. If the stack area is set to 0C0, the value of SP needs to be set to 0xBF after the system is reset.

Operations affecting SP: PUSH, LCALL, ACALL, POP, RET, RETI and access to interrupts.

The PUSH instruction occupies one byte in the stack, LCALL, ACALL and interrupt access occupy two.

Using the PUSH instruction will automatically save the current value of the operated register to RAM.

2.5 Data Pointer Register (DPTR0/DPTR1)

The data pointer is mainly used in MOVX and MOVC instructions, and its function is to locate the addresses of XRAM and ROM. There are two data pointer registers DPTR0 and DPTR1 inside the chip.

2.6 Data Pointer Selection Register (DPS)

Data Pointer Selection Register (DPS)

0x86	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DPS	ID1	ID0	TSL	AU	--	--	--	SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6	ID1-ID0:	Self-subtract/ self-add function selection.
	00=	DPTR0 plus 1 or DPTR1 plus 1;
	01=	DPTR0 minus 1 or DPTR1 plus 1;
	10=	DPTR0 plus 1 or DPTR1 minus 1;
	11=	DPTR0 minus 1or DPTR1 minus 1.
Bit5	TSL:	Flip selection enable;
	1=	After the DPTR command is executed, the SEL will flip automatically;
	0=	DPTR related instructions do not affect SEL.
Bit4	AU:	Self-add / self-subtract enable bit;
	1=	After the MOVX @ DPTR or MOVC @ DPTR instructions are allowed to run, execute self-add/self subtract(determined by ID1-ID0)
	0=	DPTR related instructions does not affect SEL.
Bit3~Bit1	--	
Bit0	SEL:	Data pointer selection bit;
	1=	Select DPTR1;
	0=	Select DPTR0.

2.7 Program Status Register (PSW)

Program Status Register (PSW)

0xD0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSW	CY	AC	F0	RS1	RS0	OV	--	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset value	0	0	0	0	0	0	0	0

Bit7 CY: Carry flag bit;
1= Carry;
0= No carry.
Bit6 AC: Auxiliary carry flag bit (half carry flag bit);
1= Carry;
0= No carry.
Bit5 F0: General-purpose flag bit.
Bit4~Bit3 RS1-RS0: Working register BANK select bit;
00= Select Bank0;
01= Select Bank1;
10= Select Bank2;
11= Select Bank3.
Bit2 OV: Overflow flag bit;
1= Arithmetic or logical operation has overflow;
0= Arithmetic or logical operation has no overflow.
Bit0 P: Parity bit;
1= The highest bit of the result is carried.
0= The highest bit of the result does not carry.

2.8 Program Counter (PC)

Program Counter (PC) controls the instruction execution sequence in the program memory Flash, Its addressing range is over the entire Flash. After obtaining the instruction code, the PC will automatically add one and point to the address of the next instruction code. But if executions such as jump, conditional jump, assign value to PCL, subroutine call, initialization reset, interrupt, interrupt return, subroutine return are performed, PC will load the address related to the instruction instead of the address of the next instruction.

When a conditional jump instruction is encountered and the jump condition is met, the next instruction which is read during the current instruction execution will be discarded, and an empty instruction operation cycle will be inserted before the correct instruction can be obtained. Otherwise, the next instruction will be executed sequentially.

2.9 Timing Access Register (TA)

Timing Access Register (TA)

0x96	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TA	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit7~Bit0 TA[7:0]: Timing access control bit.

Some protected registers must perform the following operations on TA before they can be written.

```
MOV   TA, #0AAH
MOV   TA, #055H
```

No other instructions can be inserted in the middle, and this sequence needs to be re-executed when it is modified again.

Protected registers: WDCON, CLKDIV.

2.10 Watch Dog Timer (WDT)

Watch Dog Timer is an on-chip timer, and a WDT timing overflow will result in a reset.

2.10.1 WDT Overflow Period

For details, please refer to Section 4.4 <Watchdog Reset>

2.10.2 Watch Dog Control Register (WDCON)

Watch Dog Control Register (WDCON)

0x97	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDCON	SWRST	PORF	--	--	WDTIF	WDTRF	WDTRE	WDTCLR
R/W	R/W	R/W	--	--	R/W	R/W	R/W	R/W
Reset Value	0	1	--	--	0	0	0	0

Bit7	SWRST:	Software reset control bit;
	1:	Execute system software reset (write 0 to clear after reset).
	0:	---
Bit6	PORF:	Power-on reset flag bit;
	1:	The system is power-on reset (write 0 to clear, TA write timing is not required).
	0:	---
Bit5~Bit4	Not used.	
Bit3	WDTIF:	WDT overflow interrupt flag bit;
	1=	WDT overflow (write 0 to clear);
	0=	WDT no overflow.
Bit2	WDTRF:	WDT reset flag bit;
	1=	The system is reset by WDT (write 0 to clear);
	0=	The system is not reset by WDT.
Bit1	WDTRE:	WDT Reset enable bit;
	1=	Enable WDT to reset CPU;
	0=	Disable WDT to reset CPU.
Bit0	WDTCLR:	WDT counter clear bit;
	1=	Clear WDT counter(hardware reset automatically);
	0=	Forbid WDT counter (write 0 is invalid).

Note:

1. If WDT in CONFIG is configured to enable, WDT is always enabled regardless of the state of WDTRE control bits, and the overflow reset function of WDT is forcibly turned on.
2. If WDT in CONFIG is configured to disable, WDT can be enabled or disabled by using WDTRE control bits.

The command sequence required by modifying WDCON (no other commands can be inserted in the middle):

```
MOV     TA,#0AAH
MOV     TA,#055H
ORL     WDCON,#01H
```

2.10.3 WDT Overflow Control Register (CKCON)

0x8E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CKCON	WTS2	WTS1	WTS0	T1M	T0M	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	1	1	1

Bit7~Bit5 WTS2-WTS0: WDT overflow time select bit;
000= 2^{17}*Tsys;
001= 2^{18}*Tsys;
010= 2^{19}*Tsys;
011= 2^{20}*Tsys;
100= 2^{21}*Tsys
101= 2^{22}*Tsys;
110= 2^{24}*Tsys;
111= 2^{26}*Tsys.

Bit4 T1M: Clock source selection bit for Timer1;
0= Fsys/12;
1= Fsys/4.

Bit3 T0M: Clock source selection bit for Timer0;
0= Fsys/12;
1= Fsys/4.

Bit2~Bit0 Not used.

2.11 Function Control Register (FUNCCR)

0x91	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FUNCCR	--	--	--	--	UART1_CKS1	UART0_CKS1	UART1_CKS	UART0_CKS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit4 Reserved bit: It must be 0.

Bit3 UART1_CKS1: Timer clock source higher selection bits for UART1, {UART1_CKS1, UART1_CKS}.

00= The overflow clock of Timer1;

01= The overflow clock of Timer4;

10= The overflow clock of Timer2.

11= The overflow clock of BRT;

Bit2 UART0_CKS1: Timer clock source higher selection bits for UART0, {UART0_CKS1, UART0_CKS}.

00= The overflow clock of Timer1;

01= The overflow clock of Timer4.

10= The overflow clock of Timer2;

11= The overflow clock of BRT;

Bit1 UART1_CKS: Timer clock source lower selection bits for UART1, see UART1_CKS1 description;

Bit0 UART0_CKS: Timer clock source lower selection bits for UART0, see UART1_CKS0 description;

3. SYSTEM CLOCK

3.1 System Oscillators

The chip has 4 types of oscillation:

- Internal high-speed oscillation (HSI 48MHz);
- External high-speed oscillation (HSE 8/16MHz);
- External low-speed oscillation (LSE32.768KHz);
- Internal low-speed oscillation (LSI 125KHz).

The default oscillation mode of the chip is internal high-speed oscillation, and it can be modified to other oscillators in CONFIG.

3.2 Reset Time

Reset Time refers to the time from reset to starting executing instructions of the chip. Its default design value is about 16ms. This time includes oscillator start-up time and configuration time.

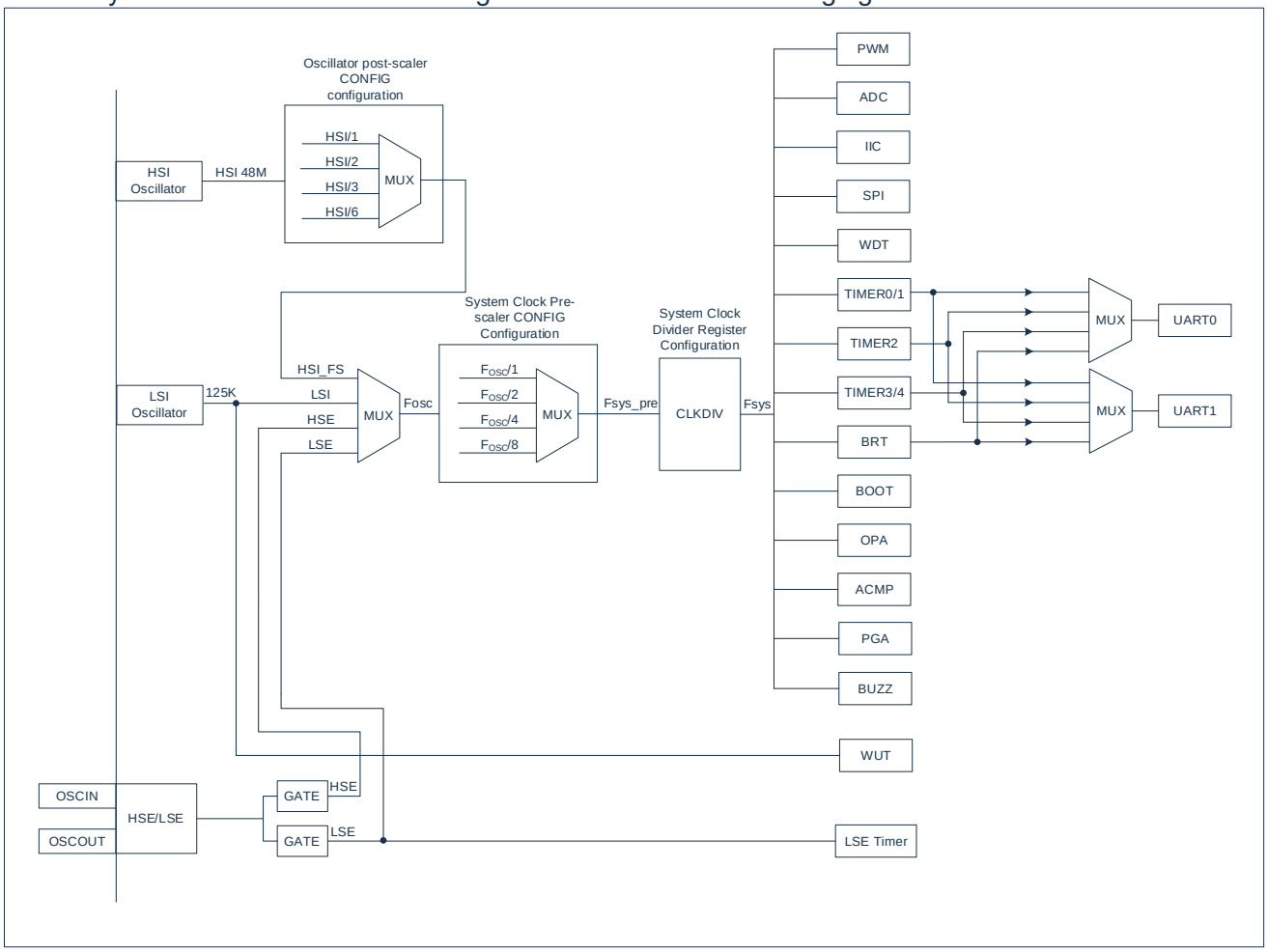
Note: This reset time will exist whether the chip is powered-on reset or reset due to other reasons.

In addition, when the oscillator is selected as external low-speed oscillation (32.768KHz), the reset time (including the start-up time) is about 1.5s as default (external capacitor is 10pF~22pF) .

3.3 Clock Structure

3.3.1 System Clock Structure

The system clock structure block diagram is shown in the following figure.



Note:
1) F_{CPU} is the clock frequency at which the CPU instructions run.
2) When the system clock oscillator is set to 1 division of HSI and Fsys_pre=Fosc/1, the F_{CPU} is fixed to Fsys/2 (24MHz).

3.3.2 Oscillator Control Register (CLKDIV)

The oscillator control register (CLKDIV) controls the system clock and frequency selection.

0x8F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKDIV	CLKDIV7	CLKDIV6	CLKDIV5	CLKDIV4	CLKDIV3	CLKDIV2	CLKDIV1	CLKDIV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 CLKDIV[7:0], Frequency division bit of system clock Fsys;
00H: Fsys=Fsys_pre;
others: Fsys =Fsys_pre/ (2*CLKDIV) (2,4…510 frequency division).

Modify the instruction sequence required by CLKDIV (no other instructions can be inserted in the middle):

```
MOV     TA,#0AAH
MOV     TA,#055H
MOV     CLKDIV,#02H
```

3.3.3 Function Clock Control Register (CKCON)

0x8E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CKCON	WTS2	WTS1	WTS0	T1M	T0M	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	1	1	1

Bit7~Bit5 WTS2-WTS0: WDT overflow time selection bit;
000= 2^{17}*Tsys;
001= 2^{18}*Tsys;
010= 2^{19}*Tsys;
011= 2^{20}*Tsys;
100= 2^{21}*Tsys
101= 2^{22}*Tsys;
110= 2^{24}*Tsys;
111= 2^{26}*Tsys.
Bit4 T1M: Clock source selection bit for Timer1;
0= Fsys/12;
1= Fsys/4.
Bit3 T0M: Clock source selection bit for Timer0;
0= Fsys/12;
1= Fsys/4.
Bit2~Bit0 Not used.

4. RESET

The chip can be reset in the following ways:

- Power-on reset;
- External reset;
- Low voltage reset;
- Watchdog overflow reset;
- Software reset;
- Internal CONFIG status protection reset;
- Power-on configuration monitoring reset.

When any of the above resets occurs, all system registers will return to the default state and the program will stop running. At the same time, the PC will be cleared and the program will start running from the reset vector 0000H after the reset.

Any kind of reset requires a certain response time, and the system provides a perfect reset process to ensure the smooth progress of the reset action.

4.1 Power-On Reset

Power-on reset is closely related to LVR operation. The power-on process of the system is in the form of a gradually rising curve, and it takes a certain time to reach the normal level. The normal timing of power-on reset is given below:

- Power on: the system detects a rise in power supply voltage and waits for it to stabilize;
- System initialization: all system registers are set to initial values;
- The oscillator starts to work: the oscillator starts to provide the system clock;
- Executing the program: the power-on is over and the program starts to run.

Stabilization time defaults to 16ms, and if 32.768KHz crystal oscillator is selected for configuration, the stabilization time is about 1.5s.

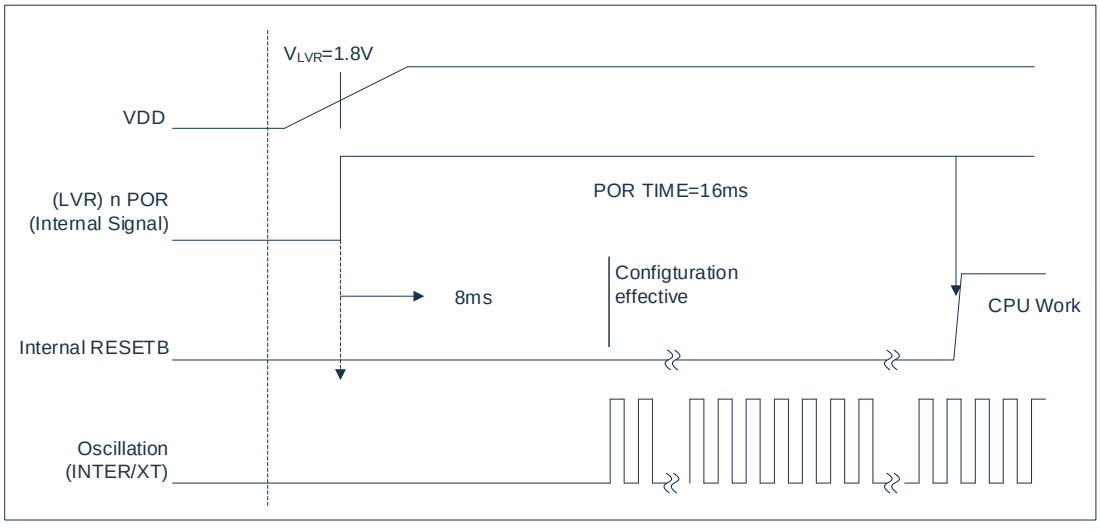


Figure 4-1: Power-on reset timing chart

Whether the system is powered on or reset can be judged by the PORF (WDCON.6) flag.

WDCON Register

0x97	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDCON	SWRST	PORF	--	--	WDTIF	WDTRF	WDTRE	WDTCLR
R/W	R/W	R/W	--	--	R/W	R/W	R/W	R/W
Reset value	0	1	--	--	0	0	0	0

Bit7 SWRST: Software reset control bit;
1: Execute system software reset (write 0 to clear after reset).
0: ---

Bit6 PORF: Power-on reset bit;
1: The system is power-on reset/LVR reset/external reset/ CONFIG protection reset (write 0 clear, no TA write timing required);
0: --

Bit5~ Bit4 Not used.

Bit3~ Bit0 WDT: Related control/flag bits. See chapter WDT for details.

The reset types that can set the PORF flag to 1 are: power-on reset, LVR reset, external reset, and CONFIG protection reset.

4.2 External Reset

External reset refers to the reset signal from the external port (NRST), which resets the chip after the Schmitt trigger input. If the NRST pin remains low for more than 16us (the internal LSI clock samples 3 rising edges) during the operating voltage range and stable oscillation, a reset is requested. After the internal state is initialized and the reset state becomes "1", it takes 16ms of stabilization time for the internal RESETB signal to become "1" and the program is executed from the vector address 0000H.

The chip re-configuration process during the stabilization time is the same as the power-on reset configuration process. The external reset pin NRST and its pull-up resistor are enabled and configured via CONFIG.

The external reset pin NRST can be configured to any external port, and the GPIO function and multiplexing function of that port are disabled after configuration.

4.3 Low Voltage Reset (LVR)

The low-voltage reset (LVR) function is integrated inside the chip. When the system voltage V_{DD} falls below the LVR voltage, the LVR is triggered and the system is reset. The voltage point that triggers the reset can be set in CONFIG.

The LVR module detects $V_{DD}<V_{LVR}$, a reset is requested.

The LVR low voltage reset function is disabled in the sleep mode (STOP) mode.

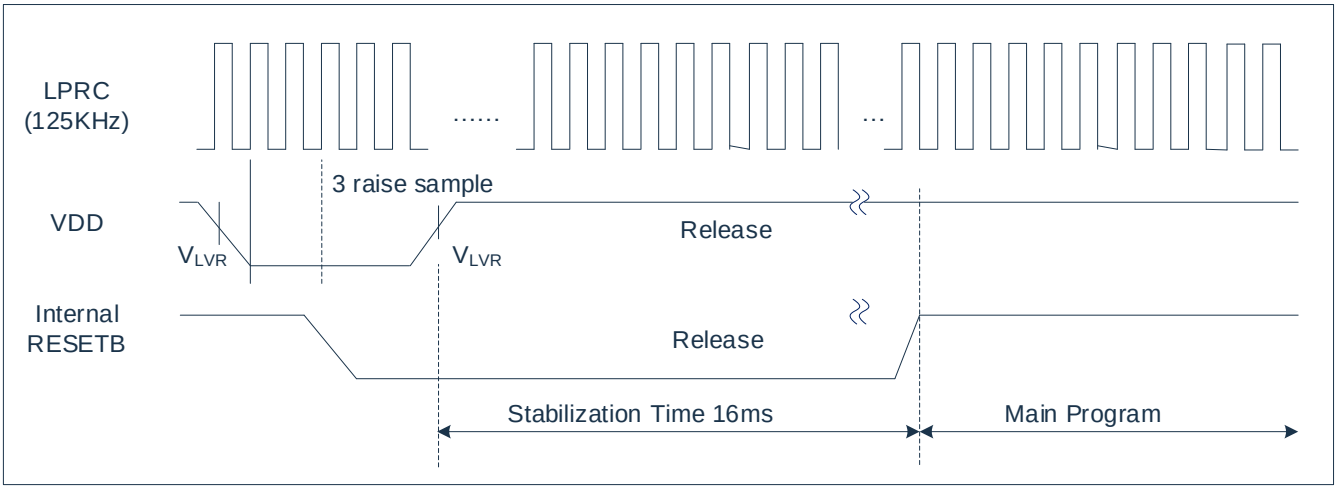


Figure 4-2: Low voltage reset timing diagram

During the stabilization time, the chip is reconfigured, which is the same as the power-on reset configuration process.

4.4 Watchdog Reset (WDT)

The watchdog reset is a protection setting for the system. In the normal state, the watchdog timer is cleared by the program. If an error occurs, the system is in an unknown state and the watchdog timer overflows and the system is reset. After the watchdog resets, the system restarts to the normal state.

The WDT counters are not addressable and start counting when the power-on reset is running. It is recommended to clear the WDT counter when setting the WDT register to accurately control the WDT time-out.

The timing of the watchdog reset is as follows:

- Watchdog timer status: the system detects if the watchdog timer overflows, and if it overflows, the system resets;
- Initialization: all system registers are set to the default state;
- Program: the reset is completed and the program starts running from 0000H.

Reset the CPU with all registers when WDT overflows, and the program is executed from 0000H immediately after 1 Tsys. WDT reset does not re-configure the power-on reset.

The clock source for the WDT is provided by the system clock, and the clock fundamental period of the WDT counter is Tsys.

The watchdog's overflow time can be set by the program. The overflow time can be selected by two bits in the CKCON register, WDS2-WTS0.

WTS[2:0]	Watchdog Interval	Number of clocks	OVT@Fsys=16MHz
000	2^{17}	131072	8.192ms
001	2^{18}	262144	16.384ms
010	2^{19}	524288	32.768ms
011	2^{20}	1048576	65.536ms
100	2^{21}	2097152	131.072ms
101	2^{22}	4194304	262.144ms
110	2^{24}	16777216	1.048s
111	2^{26}	67108864	4.194s

The WDT can also be set to not reset the system and can generate an interrupt.

4.5 Software Reset

Program software reset can be implemented inside the chip. Software reset can relocate the program flow to reset address 0000H, and then run the program again.

The user can implement a custom software reset. The control bit that implements the software reset SWRST (WDCON.7). Software reset does not reconfigure the power-on reset.

WDCON

0x97	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDCON	SWRST	PORF	--	--	WDTIF	WDTRF	WDTRE	WDTCLR
R/W	R/W	R/W	--	--	R/W	R/W	R/W	R/W
Reset value	0	1	--	--	0	0	0	0

Bit7 SWRST: Software reset control bit.
1: Execute system software reset (change from 0->1 to generate reset, software reset will not clear to zero, need to write 0 to clear).
0: ---

Bit6 PORF: Power-on reset flag.
1: The system is powered-on reset (write 0 clear, no TA write timing required).
0: --

Bit5~ Bit4 Not used.

Bit3~ Bit0 WDT related control/flag bits. See the chapter WDT for details.

4.6 CONFIG Status Protection Reset

The CONFIG state protection reset is an enhanced protection mechanism for the system. During powering on and reset, there is a set of 16-bit CONFIG registers internally that load the fixed code (A569H) set in the FLASH and are not being operated during normal operation. In the case of a specific non-program operation, the value of this register changes and does not equal to the original fixed code, after a number of sampling clocks, if the register continues to remain unfixed code, the system will reset.

This reset mechanism prevents the configuration bits from changing under certain conditions, causing the system to enter an unpredicted state.

In normal operation, the clock for sampling register value is internal RC Fixed_Clock (8MHz, clock source from HSI) and low power clock (LSI 125KHz), once the register value is not fixed code, force enable LSI oscillator and HSI oscillator, and system clock switch to LSI clock, if after 12 Fixed_ Clock sampling or 3 LSI clock sampling, the register still maintains the state of not being a fixed code, then the system generates a reset.

In order to prevent the oscillator from oscillating under certain conditions, two clocks are used for sampling.

4.7 Power-On Configuration Monitoring Reset

In the power-on configuration process, there is a configuration monitoring circuit inside the chip. If the configuration time is too long in the power-on, or if the power-on configuration enters a certain state that cannot be reconfigured, the internal monitoring circuit starts timing from the configuration, and if the set time is exceeded, the monitoring circuit resets the configuration module and allows the configuration module to re-configure the process. To prevent the system from entering a non-predictable state at power-on.

The monitoring circuit operating clock is LSI (125KHz), the default monitoring time is 65ms, if you choose 32.768KHz crystal oscillation, the monitoring time is 2.1s.

5. POWER MANAGEMENT

The low power modes are divided into 2 categories:

- IDLE: idle mode
- STOP: sleep mode

When a user is developing the program, it is strongly recommended to use the IDLE and STOP macros to control the system mode of the microcontroller. Do not set IDLE and STOP bits directly.

- Enter idle mode: IDLE();
- Enter sleep mode: STOP();

5.1 Power Management Register (PCON)

Power Management Control Register (PCON)

0x87	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD0	SMOD1	--	--	--	SWE	STOP	IDLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7	SMOD0:	UART0 baud rate multiplication bit;
	0=	UART0 baud rate is normal;
	1=	UART0 doubles the baud rate.
Bit6	SMOD1:	UART1 baud rate multiplication bit;
	0=	UART1 baud rate is normal;
	1=	UART1 doubles the baud rate.
Bit5	--	
Bit4~Bit3	Reserved bit:	It must be 0.
Bit2	SWE:	STOP status function wake-up enable bit; (The system can be restarted by a power-down reset or an enabled external reset, regardless of the SWE value)
	0=	Disable functional wake-up;
	1=	Enable function wake-up (can be woken up by external interrupt and timed wake-up)
Bit1	STOP:	The dormant state control bit;
	0=	Not in a dormant state;
	1=	Enters sleep state (automatically cleared by exiting STOP mode).
Bit0	IDLE:	Idle status control bit;
	0=	Not in idle status;
	1=	Enters idle state (automatically cleared when exiting IDLE mode).

5.2 Power Monitoring Register (LVDCON)

This MCU has its own power detection function. If the LVD module is enabled (LVDEN=1) and the voltage monitoring point LVDSEL is set at the same time, when the power supply voltage drops below the LVD setting value, an interrupt will be generated to remind the user.

If the LVD module is enabled before sleep, the hardware will not close the module circuit after entering sleep, and the software needs to be closed (LVDEN=0).

Power Monitoring Register (LVDCON)

F690H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LVDCON	--	LVDSEL[2:0]			LVDEN	--	LVDINTE	LVDINTF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7	--	
Bit6~Bit4	LVDSEL[2:0]:	LVD voltage monitoring point;
	000=	2.0V
	001=	2.2V
	010=	2.4V
	011=	2.7V
	100=	3.0V
	101=	3.7V
	110=	4.0V
	111=	4.3V
Bit3	LVDEN:	LVD module enable;
	0=	Disable;
	1=	Enable.
Bit2	--	Reserved, must be zero.
Bit1	LVDINTE:	LVD interrupt enable bit;
	0=	Disable;
	1=	Enable.
Bit0	LVDINTF:	LVD interrupt flag bit (cleared by software);
	0=	Power supply voltage is higher than the monitoring voltage;
	1=	Power supply voltage is lower than the monitoring voltage.

5.3 IDLE Mode

In this mode, only the CPU clock source is turned off. Therefore, in this state, peripheral functions (such as timers, PWM, and I^2C) and clock generators (HSI/crystal oscillator drivers) still work normally.

After the system enters the idle mode, it can be awakened by any interrupt. After waking up, it enters the interrupt processing program. After the interrupt returns, it continues to execute the instruction after the sleep operation.

If you enter the idle mode in the interrupt service routine, the system can only be awakened by the interrupt with higher priority.

5.4 STOP Mode

In this mode, all circuits except LVD module and LSE module are closed (LVD/LSE module must be closed by software), the system is in low power consumption mode, and the digital circuits are not working.

5.4.1 Wake-Up Function of STOP Mode

After entering the STOP mode, the STOP wake-up function can be enabled (SWE=1) to wake up the STOP mode. There are several ways to wake up the STOP mode.

1) INT0/1 interrupt
   Using INT0/1 interrupt wakeup STOP mode, the total interrupt enable and INT0/1 interrupt enable must be turned on before entering sleep in order to wake up the system. INT0, INT1 interrupt related registers include IE, IP, TCON, IO multiplexing mapping registers, INT0/1 interrupt wake-up can only be interrupted on the falling edge to wake up sleep.
2) External (GPIO) interrupt
   With external GPIO interrupt wake-up, the total interrupt enable and port interrupt enable must be turned on before entering sleep to wake up the system. External GPIO interrupt wake-up can be selected from rising edge, falling edge, and double-edge interrupt wake-up sleep, and the interrupt wake-up edge is set by the external interrupt control register PxnEICFG.
3) WUT timed wake-up
   The WUT timed wake-up must be turned on before going to sleep, and the time between sleep and wake-up must be set. The clock source of the WUT is provided by the LSI (Low Speed Oscillator), and the LSI is automatically turned on when the WUT is turned on.
4) LSE timed wake-up
   To wake up by LSE, the LSE module must be enabled, counted, and wake-up timed before going to sleep, and the time between sleep and wake-up must be set.

5.4.2 Wake-Up Wait State

Whether INT0 / 1 interrupt, external interrupt GPIO, or WUT timed wake-up, LSE timed wake-sleep mode, an interrupt is generated or after the regular time, we need to wait for some time to wake up the system, the next instruction execution of the program. After the interrupt is generated or the time is up, the system oscillator is started, but the oscillation frequency is not stable yet, the CPU is not working, and the PC still stops in the dormant state. The system needs to wait for a period of time before providing the clock to the CPU. The waiting time for waking up the CPU is set in the programming CONFIG, and the waiting time can be set to 50us~1s. After the wake-up waiting time has elapsed, the MCU considers that the system clock is stable, and then provides the clock to the CPU, and the program continues to execute.

If the internal wake-up timer and external interrupt wake-up function are both enabled, after the system enters the sleep mode, any wake-up method can wake up the CPU. If the internal timer wakes up the oscillator first, and then there is an external interrupt input, after the wake-up wait time has elapsed, the program executes the interrupt handler first and then continues to execute the instruction after the sleep operation.

5.4.3 Sleep Wake-Up Time

The total wake-up time using external interrupts to wake up the system is:

power manager stable time (200us)+ wake-up waiting time

The total wake-up time of the system using timing wake-up is:

power manager stable time (200us)+ wake-up timer timing+ wake-up waiting time

(The time given above is Fsys>1MHz)

5.4.4 Reset To Reboot the System

In sleep mode, the system can also be restarted by power-down reset or external reset. Regardless of the SWE value, the system can be restarted by the above reset operation even if SWE=0.

Power-down reset: without any other conditions, V_{DD} is reduced to 0V and then re-powered to the operating voltage to enter the power-up reset state.

External reset: external reset function needs to be enabled, and the relevant port is configured as a dedicated reset port. When the reset port is kept low for >1us in sleep state, the system generates a reset, and if the reset port is released, the system restarts.

5.5 Sleep Mode Application Example

Before the system enters the sleep mode, if the user needs to obtain a small sleep current, please confirm the status of all I/O first. If there is a floating I/O port in the user's application, set all the floating ports as output ports to ensure that all the input ports are set to be in fixed status. Each input port has a fixed state to prevent the increasement of the sleep current from the port line voltage level being in an indeterminate state when I/O ports are in input state; turn off other peripheral modules such as ADC module, LSE module, LVD module to reduce the sleep current.

Example: Process of entering sleep mode (assembly program)

```
SLEEP_MODE:
        MOV         IE,#00h
        MOV         P0TRIS,#0FFh
        MOV         P0,#0FFh
        MOV         P1TRIS,#0FFh
        MOV         P1,#0FFh
        MOV         P2TRIS,#0FFh
        MOV         P2,#0FFh
        MOV         P3TRIS,#0FFh
        MOV         P3,#0FFh
        Turn off other operations
        MOV         PCON,#06H       ; Perform wake-able sleep operations,
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP         ; The instruction to execute sleep operation must be followed by 6 NOP instructions
        Other intructions after wake-up
```

5.6 Sleep Power Consumption in Debug Mode

The sleep status in debug mode does not reflect the actual chip sleep status.

In debug mode, after the system enters the sleep state, the related power management circuit and the oscillator do not turn off, but continue to turn on. Wake-up operation is also possible in debug mode, and the wake-up mode is the same as normal mode.

Therefore, the sleep current obtained in this state is not the real sleep power consumption. It is recommended to close the debug mode after the sleep wake-up function is developed in debug mode, and then restart the system, the measured current at this time is the actual sleep power consumption.

6. I/O PORT

6.1 GPIO Function

The chip has four I/O ports: PORT0, PORT1, PORT2, PORT3. The readable and writable port data registers provide direct access to these ports.

PORTx is a bidirectional port. Its corresponding data direction register is PxTRIS. Setting a PxTRIS bit to 1(=1) will configure the corresponding pin as an output. Clearing a PxTRIS bit (=0) configures the corresponding PORTx pin as an input.

When PORTx is used as an output port, writing the Px register will be written to the port latch, and all write operations are read-modify-write operations. Therefore, writing a port means first reading the pin level of that port, then modifying the read value, and finally writing the modified value to the port data latch.

When PORTx is used as an output port, reading the Px register is related to the setting of the PxDS register. When one bit of PxDS is set to 1 (=1), the corresponding bit of Px is read as the state of the pin, and when one bit of PxDS is cleared (=0), the corresponding bit of Px is read as the state of the port data latch; when PORTx is used as an input port, the Px register is read as the state of the pin, independent of the setting of the PxDS register.

When using the PORTx pin as an analog input, the user must ensure that the bit in the PxTRIS register remains set to 0. I/O pins configured as analog inputs always read 0.

The registers related to PORTx port are Px, PxTRIS, PxOD, PxUP, PxRD, PxDS, etc.

6.1.1 PORTx Data Register (Px)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Px	Px7	Px6	Px5	Px4	Px3	Px2	Px1	Px0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	X	X	X	X	X	X	X	X

Register P0 address: 0x80; Register P1 address: 0x90; Register P2 address: 0xA0; Register P3 address: 0xB0.

Bit7~Bit0 Px<7:0>: Px I/O pin bit.

1= Port pin level>V_{IH};

0= Port pin level<V_{IL}.

6.1.2 PORTx Direction Register (PxTRIS)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PxTRIS	PxTRIS7	PxTRIS6	PxTRIS5	PxTRIS4	PxTRIS3	PxTRIS2	PxTRIS1	PxTRIS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register P0TRIS address: 0x9A; Register P1TRIS address: 0xA1;

Register P2TRIS address: 0xA2; Register P3TRIS address: 0xA3.

Bit7~Bit0 PxTRIS<7:0>: Tri-state control bit.

1= Pin is configured as an output;

0= The pin is configured as an input (tri-state).

Note:

1. After the port is set as the output port, the data of the port is read as the value of the output register.
2. After the port is set as the input port, the <read-modify-write> type of instruction to the port is actually the operation of the output register.

6.1.3 PORTx Open-Drain Control Register (PxOD)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PxOD	PxOD7	PxOD6	PxOD5	PxOD4	PxOD3	PxOD2	PxOD1	PxOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register P0OD address: F009H; Register P1OD address: F019H;

Register P2OD address: F029H; Register P3OD address: F039H.

Bit7~Bit0 PxOD<7:0>: Open drain control bit.

1= Pin is configured for open drain (output is open drain output);

0= Pin is configured for normal state (output is push-pull output).

6.1.4 PORTx Pull-up Resistor Control Register (PxUP)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PxUP	PxUP7	PxUP6	PxUP5	PxUP4	PxUP3	PxUP2	PxUP1	PxUP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register P0UP address: F00AH; Register P1UP address: F01AH;

Register P2UP address: F02AH; Register P3UP address: F03AH.

Bit7~Bit0 PxUP<7:0>: Pull-up resistor control bit;

1= Pin pull-up resistor is turned on;

0= Pin pull-up resistor is off.

6.1.5 PORTx Pull-Down Resistor Control Register (PxRD)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PxRD	PxRD7	PxRD6	PxRD5	PxRD4	PxRD3	PxRD2	PxRD1	PxRD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register P0RD address: F00BH; Register P1RD address: F01BH;

Register P2RD address: F02BH; Register P3RD address: F03BH.

Bit7~Bit0 PxRD<7:0>: Pull-down resistor control bit;

1= Pin pull-down resistor is turned on;

0= Pin pull-down resistor is off.

Note: The pull-down resistor control is independent of the GPIO's configuration and multiplexing functions and is controlled separately by the PxRD register.

6.1.6 PORTx Drive Current Control Register (PxDR)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PxDR	PxDR7	PxDR6	PxDR5	PxDR4	PxDR3	PxDR2	PxDR1	PxDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register P0DR address: F00CH; Register P1DR address: F01CH;

Register P2DR address: F02CH; Register P3DR address: F03CH.

Bit7~Bit0 PxDR<7:0>: Drive current control bit (valid when port is configured to output state).

1= weak driver;

0= strong driver;

6.1.7 PORTx Slope Control Register (PxSR)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PxSR	PxSR7	PxSR6	PxSR5	PxSR4	PxSR3	PxSR2	PxSR1	PxSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register P0SR address: F00DH; Register P1SR address: F01DH;

Register P2SR address: F02DH; Register P3SR address: F03DH;

Bit7~Bit0 PxSR<7:0>: Px slope control register (valid when the port is configured as output state);

1= Px pin is slow slope;

0= Px pin is fast slope.

6.1.8 PORTx Data Input Selection Register (PxDS)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PxDS	PxDS7	PxDS6	PxDS5	PxDS4	PxDS3	PxDS2	PxDS1	PxDS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register P0DS address: F00EH; Register P1DS address: F01EH;

Register P2DS address: F02EH; Register P3DS address: F03EH.

Bit7~Bit0 PxDS<7:0>: Data input selection bit, when configured as GPIO, it affects the reading of the value of Px register;

1= Output/input mode reads the pin status;
(Smit when the port is set to output state The circuit also remains open);

0= Output mode: read as the data latch status;
input mode: read as the pin status.

Note: If you need to read the pin status when the port is a multiplex function input structure, you need to set the port direction control to input mode.

6.2 Multiplexing Function

6.2.1 Port Multiplexing Function Configuration Register

PORTx Function Configuration Register (PxnCFG)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PxnCFG	--	--	--	PxnCFG4	PxnCFG3	PxnCFG2	PxnCFG1	PxnCFG0
R/W	--	--	--	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit5 -- Reserved, must be 0.

Bit4~Bit0 PxnCFG<4:0>: Function configuration bit, default is GPIO function

Please refer to Port Function Configuration for details.

There are 8 function configuration registers of Px, including Px0CFG~Px7CFG, which control the function configuration of Px0~Px7 respectively.

Each port has a function configuration register, and each port can be configured to any kind of digital function through the function configuration register PxnCFG. For example, the function configuration register of port P00 is P00CFG, and different values of the register correspond to different digital functions. For example, to set P2.4 to BEEP buzzer function, configure as follows:

Compilation: MOV #P24CFG, #18H

C: P24CFG = 0x18;

The port direction register PxTRIS does not need to be configured when the port is used for multiplexing function.

- SCL, SDA pull-up resistance register is configurable to force the open-drain output on.
- RXD0, RXD1 synchronous mode force on pull-up.

Other multiplexing functions are hardware forced to turn off the pull-up resistance and turn off the open-drain output, i.e., the pull-up resistance PxUP or open-drain output PxOD is set invalid by software.

When the port is multiplexed for SCL and SDA functions, the hardware forces the port to be an open-drain output, and the pull-up resistor PxUP can be set by software.

The numerical functions corresponding to the different configuration values are as follows:

Configuration values	Function	Direction	Function Description
0x00	GPIO	I/O	General-purpose IO port, configure input and output, pull-up and pull-down, etc. via registers
0x01	ANALOG		Analog function
0x02	--	--	--
0x03	--	--	--
0x04	CC0	O	Timer2 compare output channel 0
0x05	CC1	O	Timer2 compare output channel 1
0x06	CC2	O	Timer2 compare output channel 2
0x07	CC3	O	Timer2 compare output channel 3
0x08	TXD0	O	UART0 data output
0x09	RXD0	I/O	UART0 data input / synchronous mode data output

Configuration values	Function	Direction	Function Description
0x0A	TXD1	O	UART1 data output
0x0B	RXD1	I/O	UART1 data input / synchronous mode data output
0x0C	SCL	I/O	I^2C clock input and output
0x0D	SDA	I/O	I^2C data input and output
0x0E	NSS	I/O	SPI slave mode chip select signal (input/output)
0x0F	SCLK	I/O	SPI clock input and output
0x10	MOSI	I/O	SPI master send slave receive
0x11	MISO	I/O	SPI master receive slave transmit
0x12	PG0	O	PWM channel 0 output
0x13	PG1	O	PWM channel 1 output
0x14	PG2	O	PWM channel 2 output
0x15	PG3	O	PWM channel 3 output
0x16	PG4	O	PWM channel 4 output
0x17	PG5	O	PWM channel 5 output
0x18	BEEP	O	Buzzer output
0x19	--	--	--
0x1A	C0_O	O	Comparator 0 output
0x1B	C1_O	O	Comparator 1 output
0x1C	--	--	--
0x1D	--	--	--
0x1E	--	--	--
0x1F	--	--	--

Note:

1) The configuration values marked as "--" in the table are reserved and disabled.
2) The function configuration register is 0x00 by default, and the port is used as GPIO function. Different functions can be set by GPIO function register in chapter 6.1.
3) When the function configuration register is set to 0x01, the hardware turns off the digital circuitry to reduce power consumption and the GPIO function-related register setting is disabled. The port supports multiple analog functions, as described in the following table.
4) There is no restriction on the priority order of the ports that are used as output functions in the multiplexing function. If there are multiple ports configured for the same output function, the function will be output on those ports at the same time.
5) The ports used as input functions in the multiplexing function are restricted in priority order. If there are two or more ports configured with the same input function at the same time, the selection is configured in the order of priority from highest to lowest for P0.0, P0.1, ..., P3.2, and P3.5.
   If P00 and P32 are configured as RXD0 port at the same time: P00CFG = 0x09; P32CFG = 0x09. Since P0.0 has a higher priority, the RXD0 source is actually connected to the input of port P0.0 and will not be used as the RXD0 source even if there is a data waveform at port P3.2.

The corresponding analog functions of the ports are as follows.

PIN	CONFIG	0 (GPIO)	1(ANALOG)				Other digital function priority
P0.0			AN0	C0P1			Highest
P0.1			AN1	C0P2			
P0.2			AN2	C1P2			
P0.3			AN3	C1P1			
P0.4			AN4	C1P0			
P0.5			AN5	C1N			
P1.3			AN6	C0P0			
P1.4			AN7	C0N			
P1.5			AN18				
P1.6			AN19				
P1.7			AN20				
P2.1	DSCK		AN21				
P2.2			AN8		OP1_P		
P2.3			AN9		OP1_N		
P2.4			AN10	C0P5/C1P5	OP1_O		
P2.5			AN11				
P2.6			AN12			PGATO	
P3.0			AN22	C0P4/C1P4	OP0_O		
P3.1	OSCIN		AN13		OP0_N	PGAP	
P3.2	OSCOUT		AN14		OP0_P	PGAGND	
P3.5	DSDA		AN16				
P3.6			AN17				Minimum

6.2.2 Port Input Function Allocation Register

There are digital functions with only input status inside thechip, such as INT0/INT1... etc. This type of digital input function has nothing to do with the port multiplexing status. As long as the assigned port supports digital input (such as RXD0 as a digital input and GPIO as an input function), the port supports this function.

The input function port allocation register is as follows:

Input function configuration register	Address	Function	Description
PS_INT0	F0C0H	INT0	External interrupt 0 input port allocation register
PS_INT1	F0C1H	INT1	External interrupt 1 input port allocation register
PS_T0	F0C2H	T0	Timer0 external clock input port allocation register
PS_T0G	F0C3H	T0G	Timer0 gate input port Assign register
PS_T1	F0C4H	T1	Timer1 external clock input port assignment register
PS_T1G	F0C5H	T1G	Timer1 gate control input port assignment register
PS_T2	F0C6H	T2	Timer2 external event or gate control input port assignment register
PS_T2EX	F0C7H	T2EX	Timer2 falling edge automatic reload input port assignment register
PS_CAP0	F0C8H	CAP0	Timer2 input capture channel 0 port allocation register
PS_CAP1	F0C9H	CAP1	Timer2 input capture channel 1 port allocation register
PS_CAP2	F0CAH	CAP2	Timer2 input capture channel 2 port allocation register
PS_CAP3	F0CBH	CAP3	Timer2 input capture channel 3 port allocation register
PS_ADET	F0CCH	ADET	ADC external trigger input port allocation register
PS_FB	F0CDH	FB	PWM external brake signal input port allocation register

PS_XX Input Function Port Allocation Register PS_XX (as described in the above table)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS_XX	--	--	PS_XX5	PS_XX4	PS_XX3	PS_XX2	PS_XX1	PS_XX0
R/W	--	--	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit7~Bit6 --: Reserved, must be 0

Bit5~Bit0 PS_XX<5:0>: Input function allocation control bit
(subject to the actual port of the chip, unused values are reserved and prohibited).

0x00= Allocated to port P00.
0x01= Allocated to port P01.
....
0x14= Allocated to port P14.
0x15= Allocated to port P15.
....
0x35= Allocated to port P35.
0x36= Allocated to port P36.
....
0x3F= Not assigned to a port.

1) This input function assignment structure supports multiple input functions assigned to the same port. For example, INT0 and CAP0 can be assigned to port P00 at the same time, with the following configuration.
   P00CFG = 0x00;//P00 port is configured for GPIO function
   P0TRIS = 0x00;//P00 for GPIO input function
   PS_INT0 = 0x00;//P00 port is configured for INT0 function
   PS_CAP0 = 0x00;//P00 port is configured for CAP0 function
2) This input function assignment structure is relatively independent and can support simultaneous use with other multiplexed function ports, at this time there is no need to configure the direction register of the corresponding port, such as RXD0 and INT0 can be assigned to the P00 port at the same time, configured as follows:
   P00CFG = 0x09;//P00 port is configured for RXD0 function of UART0
   PS_INT0 = 0x00;//P00 port is configured for INT0 function
3) This input function configuration structure can also be used simultaneously with the external interrupt function of the port. For example, both CAP0 and GPIO interrupt functions can be assigned to the P00 port, configured as follows.
   P00CFG = 0x00;//P00 port is configured for GPIO function
   P0TRIS = 0x00;//P00 for GPIO input function
   PS_CAP0 = 0x00;//P00 port is configured for CAP0 function
   P00EICFG = 0x01;//P00 port is configured for rising edge triggered interrupt
   P0EXTIE = 0x01;//Enable external interrupt of port P00

6.2.3 Port External Interrupt Control Register

When using external interrupts, the port needs to be configured as a GPIO function and the direction is set as an input port. Or the multiplexing function is an input port (such as RXD0, RXD1).

PORTx External Interrupt Control Register (Px_NEICFG)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Px_NEICFG	--	--	--	--	--	--	Px1EICFG1	Px0EICFG0
R/W	--	--	--	--	--	--	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit2 Not used.

Bit1~Bit0 Px_NEICFG<1:0>: P_{xN} external interrupt control bit;

00= External interrupt disabled;

01= Rising edge trigger interrupt;

10= Falling edge trigger interrupt;

11= Rising edge or falling edge trigger interrupt.

There are 8 external interrupt control registers of Px, including Px0EICFG~Px7EICFG, which control the external interrupts of Px0~Px7 respectively.

6.2.4 Cautions on the Application of Multiplexing Functions

1) The input of the multiplexing function is relatively independent of the external interrupt (GPIO interrupt) of the port and the structure of the port input function.
   For example, configure the P01 port as RXD0, and configure the P01 GPIO interrupt trigger mode as rising edge trigger and interrupt enable. When the P01 input changes from low to high, it will trigger the P01 GPIO interrupt.
2) The input structure of the digital signal is not affected by the system configuration status.
   For example, if the P01 port is powered on and configured as an external reset port, the input module of this port will be opened. If P01 is configured as INT0 in the program and the interrupt enable is turned on, the interrupt service routine will be executed before the reset signal sampling time is valid, and then the reset operation will be generated.
3) It should be noted that in the debug mode, if the multiplexing function is configured on the DSDA port, the input function is also valid. It is recommended that the related multiplexing function is not configured to the DSDA port in the debugging mode.

7. INTERRUPT

7.1 Overview

The chip has 21 interrupt sources and interrupts vectors:

Interrupt sources	Interrupt description	Interrupt vectors	Same priority sequence
INT0	External Interrupt 0	0-0x0003	1
Timer0	Timer 0 interrupt	1-0x000B	2
INT1	External interrupt 1	2-0x0013	3
Timer1	Timer 1 interrupt	3-0x001B	4
UART0	TI0or RI0	4-0x0023	5
Timer2	Timer 2 interrupt	5-0x002B	6
UART1	TI1or RI1	6-0x0033	7
P0EXTIF<7:0>	P0 port external interrupt	7-0x003B	8
P1EXTIF<7:0>	P1 port external interrupt	8-0x0043	9
P2EXTIF<7:0>	P2 port external interrupt	9-0x004B	10
P3EXTIF<7:0>	P3 port external interrupt	10-0x0053	11
--	--	11-0x005B	12
LVD	LVD power-down interrupt	12-0x0063	13
LSE_Timer	LSE Timer Interrupt	13-0x006B	14
ACMP	Comparator interrupt	14-0x0073	15
Timer3	Timer 3 interrupt	15-0x007B	16
Timer4	Timer 4 interrupt	16-0x0083	17
--	--	17-0x008B	18
PWM	PWM interrupt	18-0x0093	19
ADC	ADC interrupt	19-0x009B	20
WDT	WDT interrupt	20-0x00A3	21
I^2C	I^2C interrupt	21-0x00AB	22
SPI	SPI Interrupt	22-0x00B3	23

The chip specifies two interrupt priorities to achieve two-level interrupt nesting.

When an interrupt has already responded, if a advanced interrupt sends a request, the latter can interrupt the former and implement interrupt nesting. However, the same level or lower level interrupt can not interrupt the advanced interrupt response.

7.2 External Interrupt

7.2.1 INT0/INT1 Interrupt

The chip supports the 8051's original INT0, INT1 external interrupts, INT0/INT1 can choose falling edge or low level to trigger interrupt, and the related control register is TCON. INT0 and INT1 occupy two interrupt vectors.

7.2.2 GPIO Interrupt

Each GPIO pin of the chip supports external interrupts. And can support falling edge/rising edge/double edge interrupt. To choose which edge to trigger in PxN EICFG register configuration, example: if you need to configure P1.3 port as falling edge interrupt:

```
P13CFG=0x00;      //set P1.3 as GPIO
P1TRIS&=0xF7;     //set P1.3 as input port
P13EICFG=0x02;    //set P1.3 as falling edge triggered interrupt
```

The interrupts of GPIO occupy a total of 4 interrupt vectors:

- P0.0-P0.5 occupy an interrupt vector 0x003B;
- P1.3-P1.7 occupy an interrupt vector 0x0043;
- P2.1-P2.6 occupy an interrupt vector 0x004B;
- P3.0-P3.2, P3.5-P3.6 occupy an interrupt vector 0x0053.

If an interrupt is generated, entering the interrupt service program can first determine which port triggered the interrupt, and then process it accordingly.

7.2.3 Interrupt and Sleep Wakeup

Each external interrupt can be set to wake up the system after it enters the sleep mode (STOP wake-able mode).

INT0/INT1 interrupt wake-up system needs to open the corresponding interrupt enable and total interrupts enable, and wake-up mode is falling edge wake-up (INT0/INT1 wake-up mode and interrupt trigger mode selection bit IT0/IT1 are not related).

GPIO interrupt wake-up system, it is recommended to set the corresponding port interrupt trigger edge mode (GPIO wake-up mode is the same as interrupt trigger edge mode, you can choose rising edge/falling edge/double edge wake-up), as well as turn on the corresponding interrupt enable and total interrupts enable before entering the modification mode.

After the system is woken up by an external interrupt, it firstly enters the interrupt service program to handle the interrupt wake-up task, and after exiting the interrupt service program, the system continues to execute the instructions after the sleep operation.

7.3 Interrupt Register

7.3.1 Interrupt Mask Register

IE Interrupt Mask Register IE is a readable and writable register that can be operated by bit.

When an interrupt condition occurs, the interrupt flag will be set, regardless of the corresponding interrupt enable bit or the state of the global enable bit EA (in the IE register). User software should ensure that the corresponding interrupt flag bit is cleared before allowing an interrupt.

Interrupt Mask Register (0xA8)

0xA8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 EA: Overall interrupt enable bit;
1= Enable all un-masked interrupt;
0= Disable all interrupt.

Bit6 ES1: UART1 interrupt enable bit;
1= Enable UART1 interrupt;
0= Disable UART1 interrupt.

Bit5 ET2: TIMER2 interrupt enable bit;
1= Enable TIMER2 interrupt;
0= Disable TIMER2 interrupt.

Bit4 ES0: UART0 interrupt enable bit;
1= Enable UART0 interrupt;
0= Disable UART0 interrupt.

Bit3 ET1: TIMER1 interrupt enable bit;
1= Enable TIMER1 interrupt;
0= Disable TIMER1 interrupt.

Bit2 EX1: External interrupt 1 enable bit;
1= Enable external interrupt 1;
0= Disable external interrupt 1.

Bit1 ET0: TIMER0 interrupt enable bit;
1= Enable TIMER0 interrupt;
0= Disable TIMER0 interrupt.

Bit0 EX0: External interrupt 0 enable bit;
1= Enable external interrupt 0;
0= Disable external interrupt 0.

Timer2 Interrupt Mask Register T2IE (0xCF)

0xCF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2IE	T2OVIE	T2EXIE	--	--	T2C3IE	T2C2IE	T2C1IE	T2C0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 T2OVIE: Timer2 overflow interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit6 T2EXIE: Timer2 external load interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit5 --
Bit4 --
Bit3 T2C3IE: Timer2 compare3 interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit2 T2C2IE: Timer2 compare2 interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit1 T2C1IE: Timer2 compare1 interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit0 T2C0IE: Timer2 compare0 interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.

If Timer2 interrupt is enabled, the total interrupt enable bit of Timer2 must be enabled. ET2=1 (IE.5=1)

P0 port interrupts control register P0EXTIE (0xAC)

0xAC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0EXTIE	--	--	P05IE	P04IE	P03IE	P02IE	P01IE	P00IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --
Bit5~Bit0 P0iIE: P0i port interrupt enable bit (i=0-5);
1= Enable interrupt;
0= Disable interrupt;

P1 Port Interrupt Control Register P1EXTIE (0xAD)

0xAD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1EXTIE	P17IE	P16IE	P15IE	P14IE	P13IE	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit3 P1iIE: P1iport interrupt enable bit (i =3-7);
1= Enable interrupt;
0= Disable interrupt.
Bit2~Bit0 --

P2 Port Interrupt Control Register P2EXTIE (0xAE)

0xAE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2EXTIE	--	P26IE	P25IE	P24IE	P23IE	P22IE	P21IE	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 --
Bit6~Bit1 P2iIE: P2iport interrupt enable bit (i=1-6);
1= Enable interrupt;
0= Disable interrupt.
Bit0 --

P3 Port Interrupt Control Register P3EXTIE (0xAF)

0xAF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P3EXTIE	--	P36IE	P35IE	--	--	P32IE	P31IE	P30IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 --
Bit6~Bit5 P3iIE: P3iport interrupt enable bit (i=5-6);
1= Enable interrupt;
0= Disable interrupt.
Bit4~Bit3 --
Bit2~Bit0 P3iIE: P3iport interrupt enable bit (i=0-2);
1= Enable interrupt;
0= Disable interrupt.

Interrupt Mask Register EIE2 (0xAA)

0xAA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIE2	SPIIE	I2CIE	WDTIE	ADCIE	PWMIE	--	ET4	ET3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPIIE: SPI Interrupt enable bit
1= Enable SPI interrupt;
0= Disable SPI interrupt.
Bit6 I2CIE: I^2C Interrupt enable bit
1= Enable I^2C interrupt;
0= Disable I^2C interrupt.
Bit5 WDTIE: WDT Interrupt enable bit
1= Enable WDT interrupt;
0= Disable WDT interrupt.
Bit4 ADCIE: ADC Interrupt enable bit
1= Enable ADC interrupt;
0= Disable ADC interrupt.
Bit3 PWMIE: PWM global interrupt enable bit
1= Enable PWM global interrupt;
0= Disable PWM global interrupt.
Bit2 --
Bit1 ET4: Time4 Interrupt enable bit
1= Enable Time4 interrupt;
0= Disable Time4 interrupt.
Bit0 ET3: Time3 Interrupt enable bit
1= Enable Time3 interrupt;
0= Disable Time3 interrupt.

7.3.2 Interrupt Priority Control Register

Interrupt priority control register IP is a readable and writable register that can be operated bit by bit.

Interrupt priority control register IP (0xB8)

0xB8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IP	--	PS1	PT2	PS0	PT1	PX1	PT0	PX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 --

Bit6 PS1: UART1 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt;

Bit5 PT2: TIMER2 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit4 PS0: UART0 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit3 PT1: TIMER1 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit2 PX1: External interrupt 1 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit1 PT0: TIMER0 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit0 PX0: External interrupt 0 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Port Interrupt Priority Control Register EIP1 (0xB9)

0xB9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIP1	PACMP	PLSE	PLVD	--	PP3	PP2	PP1	PP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 PACMP: Analog comparator interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit6 PLSE Low-speed crystal timer interrupt priority control bit
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit5 PLVD LVD voltage monitoring interrupt priority control bit
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit4 --

Bit3 PP3: P3 port interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit2 PP2: P2 port interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit1 PP1: P1 port interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit0 PP0: P0 port interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Peripheral Interrupt Priority Control Register EIP2 (0xBA)

0xBA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIP2	PSPI	PI2C	PWDT	PADC	PPWM	--	PT4	PT3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 PSPI: SPI interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.
Bit6 PI2C: I^2C interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.
Bit5 PWDT: WDT interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.
Bit4 PADC: ADC interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.
Bit3 PPWM: PWM interrupt priority control bit
1= Set to advanced interrupt;
0= Set to low level interrupt.
Bit2 --
Bit1 PT4: TIMER4 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.
Bit0 PT3: TIMER3 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

7.3.3 Interrupt Flag Bit Register

Timer0/1, INT0/1 interrupt flag bit register TCON, can perform addressing by bit.

0x88	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 TF1: Timer1 counter overflows the interrupt flag bit;
1= Timer1 counter Overflow, enter the interrupt service program hardware automatically zero;
0= Timer1 counter has no overflow.

Bit6 TR1: Timer1 runs the control bit;
1= Timer1 starts;
0= Timer1 stopped.

Bit5 TF0: Timer0 counter overflows the interrupt flag bit;
1= Timer0 enter the interrupt service program hardware automatically zero;
0= Timer0 counter has no overflow.

Bit4 TR0: Timer0 runs the control bit;
1= Timer0 starts;
0= Timer0 stopped.

Bit3 IE1: External interrupt 1 flag bit;
1= External interrupt 1 produces an interrupt, and the hardware of the interrupt service program is automatically cleared;
0= External interrupt 1 did not cause an interrupt.

Bit2 IT1: External interrupt 1 trigger mode control bit;
1= The falling edge triggers;
0= Low-level trigger.

Bit1 IE0: External interrupt 0 flag bit;
1= External interrupt 0 produces an interrupt, and the hardware of the interrupt service program is automatically cleared.
0= External interrupt 0 did not cause an interrupt.

Bit0 IT0: External interrupt 0 trigger mode control bit;
1= The falling edge triggers;
0= Low-level trigger.

UART0 interrupt flag bit register SCON0, can perform addressing by bit.

0x98	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON0	U0SM0	U0SM1	U0SM2	U0REN	U0TB8	U0RB8	TI0	RI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit2 U0SM0, U0SM1, U0SM2, U0REN, U0TB8, U0RB8:UART related control bits, see UART0 function description.

Bit1 TI0: UART0 sends interrupt flag bits;

1= Synchronous mode ends at the eighth bit, or sends the stop bit asynchronously. Software can also clear it to zero.

0= ---

Bit0 RI0: UART0 receives interrupt flag bits;

1= Synchronous mode received the eighth bit, or asynchronous received. Software can also clear it to zero.

0= ---

TI0 and RI0 occupy the same interrupt vector (0023H) and require a query to determine whether to receive an interrupt or send an interrupt.

UART1 interrupt flag bit register SCON1, this register can not perform addressing by bit

0xEA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON1	U1SM0	U1SM1	U1SM2	U1REN	U1TB8	U1RB8	TI1	RI1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit2 U1SM0, U1SM1, U1SM2, U1REN, U1TB8, U1RB8: UART1 related control bit, see UART1 function description

Bit1 TI1: UART1 sends interrupt flag bits.

1= Synchronous mode ends at the eighth bit, or sends the stop bit asynchronously. Software can also clear it to zero.

0= ---

Bit0 RI1: UART1 receives interrupt flag bits;

1= Synchronous mode received the eighth bit, or asynchronous received. Software can also clear it to zero.

0= ---

TI1 and RI1 occupy the same interrupt vector (0033H) and require a query to determine whether to receive an interrupt or send an interrupt.

Timer2 Interrupt Flag Bit Register T2IF (0xC9)

0xC9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2IF	TF2	T2EXIF	--	--	T2C3IF	T2C2IF	T2C1IF	T2C0IF
R/W	R/W	R/W	--	--	R/W	R/W	R/W	R/W
Reset value	0	0	--	--	0	0	0	0

Bit7 TF2: Timer2 counter overflow interrupt flag bit;
1= The Timer2 counter overflows and needs to be cleared by software;
0= Timer2 counter has no overflow.
Bit6 T2EXIF: Timer2 external load flag bit;
1= Timer2's T2EX port generates a falling edge and needs to be cleared by software;
0= --
Bit5 --
Bit4 --
Bit3 T2C3IF: Timer2 compares the channel 3 flag bit;
1= Timer2 compares channel 3 {CCH3:CCL3}={TH2.TL2} and needs to be cleared by software.
0= ---
Bit2 T2C2IF: Timer2 compares the channel 2 flag bit;
1= Timer2 compares channel 2 {CCH2:CCL2}={TH2.TL2} and needs to be cleared by software.
0= ---
Bit1 T2C1IF: Timer2 compares the channel 1 flag bit;
1= Timer2 compares channel 1 {CCH1:CCL1}={TH1.TL1} and needs to be cleared by software.
0= ---
Bit0 T2C0IF: Timer2 compares the channel 0 flag bit;
1= Timer2 compares channel 0 {RLDH:RLDL}={TH2.TL2} and needs to be cleared by software.
0= ---

P0 Interrupt Flag Bit Register P0EXTIF (0xB4)

0xB4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0EXTIF	--	--	P05IF	P04IF	P03IF	P02IF	P01IF	P00IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --
Bit5~Bit0 P0iIF: P0i port interrupt flag bit (i=0-5);
1= P0i port generate an interrupt and need to be cleared by software;
0= No interrupt is generated at P0i port.

P1 Interrupt Flag Bit Register P1EXTIF (0xB5)

0xB5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1EXTIF	P17IF	P16IF	P15IF	P14IF	P13IF	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit3 P1iIF: P1i port interrupt flag bit (i=3-7);
1= P1i port generate an interrupt and need to be cleared by software;
0= No interrupt is generated at P1i port
Bit2~Bit0 --

P2 Interrupt Flag Bit Register P2EXTIF (0xB6)

0xB6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2EXTIF	--	P26IF	P25IF	P24IF	P23IF	P22IF	P21IF	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 --
Bit6~Bit1 P2[i]IF: P2[i] port interrupt flag bit (i=1-6);
1= P2[i] port generate an interrupt and need to be cleared by software;
0= No interrupt is generated at P2[i] port
Bit0 --

P3 Interrupt Flag Bit Register P3EXTIF (0xB7)

0xB7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P3EXTIF	--	P36IF	P35IF	--	--	P32IF	P31IF	P30IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 --
Bit6~Bit5 P3[i]IF: P3[i] port interrupt flag bit (i=5-6);
1= P3[i] port generate an interrupt and need to be cleared by software;
0= No interrupt is generated at P3[i] port.
Bit4~Bit3 --
Bit2~Bit0 P3[i]IF: P3[i] port interrupt flag bit (i=0-2);
1= P3[i] port generate an interrupt and need to be cleared by software;
0= No interrupt is generated at P3[i] port.

External Interrupt Flag Bit Register EIF2 (0xB2)

0xB2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIF2	SPIIF	I2CIF	--	ADCIF	PWMIF	--	TF4	TF3
R/W	R	R	--	R/W	R	--	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPIIF: SPI total interrupt instruction, Read only;
1= SPI interrupt.(Automatically cleared after clearing the specific interrupt flag);
0= No SPI interrupt.
Bit6 I2CIF: I^2C Total interrupt instruction, Read only;
1= I^2C interrupt, (Automatically cleared after clearing the specific interrupt flag);
0= No I^2C interrupt.
Bit5 --
Bit4 ADCIF: ADC interrupt flag;
1= ADC Conversion completed, need software clear;
0= ADC conversion is not complete.
Bit3 PWMIF: PWM Total interrupt instruction, Read only;
1= PWM interrupt, (Automatically cleared after clearing the specific interrupt flag);
0= No PWM interrupt.
Bit2 --
Bit1 TF4: Timer4 counter overflow interrupt flag;
1= Timer4 enter the interrupt service routine, the hardware automatically clears;
0= Timer4 counter has no overflow.
Bit0 TF3: Timer3 counter overflow interrupt flag;
1= Timer3 enter the interrupt service routine, the hardware automatically clears;
0= Timer3 counter has no overflow.

SPI Interrupt Flag Bit Register SPSR (0xED)

0xED	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPSR	SPISIF	WCOL	--	--	--	--	--	SSCEN
R/W	R	R	--	--	--	--	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPISIF: SPI complete flag, Read only;
1= SPI transfer to complete (Read SPSR first, then clear after reading/writing SPDR);
0= SPI not transferred.
Bit6 WCOL: SPI Write conflict error flag Read only;
1= SPI Write conflict error (Read SPSR first, then clear after reading/writing SPDR);
0= No Write conflict error.
Bit5 --
Bit4 --
Bit3~Bit2 --
Bit1 Reserved: Must be 0
Bit0 SSCEN: SPI master control mode NSS output control bit.
1= NSS outputs high when SPI is being in idle state;
0= NSS outputs the content of register SSCR.

I²C Master Interrupt Flag Bit Register I2CMCR/I2CMSR

0xF5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CMCR	RSTS	--	--	--	ACK	STOP	START	RUN
I2CMSR	I2CMIF	BUS_BUSY	IDLE	ARB_LOST	DATA_ACK	ADDR_ACK	ERROR	BUSY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 RSTS: I²C active module reset control bit;
1= Reset the master module (I² C registers of the entire master module, including I2CMSR);
0= I²C Interrupt flag bit cleared to 0 in master control mode.
I2CMIF: I²C interrupt flag bit in master mode;
1= Send/receive complete in master mode, or a transmission error occurs. (software clear, write 0 to clear);
0= No interruptions were generated.
Bit6~Bit0 I²C Control and flag bits in master control mode, see I2CM description for details.

I²C Slave Status Register I2CSSR

0xF2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CSSR	--	--	--	--	--	SENDFIN	TREQ	RREQ
R/W	--	--	--	--	--	R	R	R
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit3 --
Bit2 SENDFIN: Sending complete flag bit in I²C slave mode (read only).
1= The master control device no longer needs data, the TREQ is no longer set to 1, and the data transmission has been completed.(automatically cleared after reading I2CSCR)
0= ---
Bit1 TREQ: Prepared sending flag bit In I²C slave mode (read only).
1= As the transmitting device is already addressed or the master device is ready to receive data. (automatically cleared to zero after writing I2CSBUF)
0= ---
Bit0 RREQ: Receiving complete flag bit In I²C slave mode (read only).
1= Receive complete. (automatically write zero after reading I2CSBUF)
0= Uncompleted.

The related state bit of the I²C slave mode is also the interrupt flag bit.

Note: I2C master mode interrupt and active interrupt share the same interrupt vector(00ABH).

7.3.4 Clearance of Interrupt Flag Bit

The clearance of interrupt flag bits in the system is divided into the following steps:

- Hardware auto-clear (requires access to interrupt service program)
- Software clear
- Read/write to clear

1) Flag bits automatically cleared by hardware
   The bits that support hardware auto clear are the interrupt flag bits generated by INT0, INT1, T0, T1, T3, and T4. The hardware auto clear flag conditions are: turn on the total interrupt enable bit EA=1 and turn on the corresponding interrupt enable bit, after generating an interrupt the system enters the corresponding interrupt service program and the flag bits are cleared automatically. If the interrupt enable is turned off, these flag bits can also be cleared using the software.
2) Flag bits cleared by software
   There are flag bits in the system that can only be cleared by software. These flags are not automatically cleared after entering the interrupt service program and require a software write 0 to clear them. Otherwise, they will enter the interrupt service program again after exiting the interrupt service program.
3) Flag bits cleared by read and write operations
   There are flag bits in the system that do not write 0 to that flag bit to clear it, but need to read/write other registers to clear the flag bit. For example, the transfer completion flag bit SPISIF in the SPI interrupt flag register, after setting 1, you need to read SPSR and then read/write SPDR to clear it.

The software clear operation needs to be noted that when multiple interrupt flags are in the same register and the moments when these flags are generated are not related to each other, it is not recommended to use the read-modify-write operation.

For example, the PWMUIF interrupt flag bit register, which contains the upward comparison interrupts of channels PG0-PG5, these interrupt flag bits are not related to each other. When PG0 generates an upward comparison interrupt, the value of PWMUIF is 0x01, and the bit is cleared by a read-modify-write operation after entering the interrupt service program.

```
PWMUIF &= 0xFE;
```

This operation is implemented by first reading the value of PWMUIF back to the CPU and then performing the operation, and finally sending it back to P WMUIF. If the interrupt flag bit PWMUIF[1] of PG1 is set to 1 after the CPU reads it, and PWMUIF[1] is 0 when it is read, then it is also 0 when it is sent back to PWMUIF[1] after the operation. At this time, the up interrupt flag bit PWMUIF[1] already generated by PG1 is cleared.

To clear the interrupt flag bits of the above types, it is recommended to write 0 directly and 1 for other irrelevant flag bits:

```
PWMUIF = 0xFE;
```

Writing 1 to the irrelevant interrupt flag bits has no practical effect.

7.3.5 Special Interrupt Flag Bits in Debug Mode

The flag bit in the system does not write 0 to the flag bit zero, but needs to read/write other registers to clear the flag bit.

In the test state, the Breakpoint is executed, and after the single step operation or stop operation, the emulator will read the value of all registers from the system to the simulation software. The read/write operation of the emulator is exactly the same as read/write in normal mode.

Therefore, during debugging, after a pause occurs, an interrupt flag bit of 1 should appear, but it is displayed as 0 in the observation window.

Example: SPI interrupt flag bit register transmission completed flag bit SPISIF in debug mode

```
...                                 // Set port and interrupt enable
SPDR = 0x56;                  // Send SPDR data
delay();
...

void SPI_int (void) interrupt SPI_VECTOR     // SPI interrupting service procedures
{
        O1  _nop_();          // Set Breakpoint 1
            _nop_();
        O2  k = SPSR;      //  Set Breakpoint 2
            _nop_();
        ...
}
```

When the Breakpoint is running, after the SPI stops at Breakpoint 1, the SPI completes the send operation and has generated a send completion interrupt, so SPSR .7 = 1, at which point the emulator has completed reading all the hosting operations (including reading SPSR).

Run the Breakpoint again and stop at Breakpoint 2. At this point, the emulator completes reading all registers (including SPDR) again, so SPSR .7 = 0 at this time. The above situation can also occur twice in a single step, and you need to pay attention in debugging mode.

8. LSE TIMER

8.1 Overview

LSE timer is a 16-bit up-counting timer with a clock source from the external low-speed clock LSE. When using the LSE timer function, you should first set the LSE module to be enabled, wait for the LSE clock to stabilize (about 1.5s), and then set the LSE count enable. The timer adds 1 to the count value at the rising edge of the LSE clock. When the count value is equal to the timing value, the interrupt flag bit LSECON[0] is set to 1, and the counter starts counting from 0 again. The timing value is set by the register {LSECRH[7:0], LSECRL[7:0]}.

If the LSE timing function is configured before sleep, the LSE oscillator and LSE timer can continue to work when the chip sleeps without being affected. If the LSE timer wake-up function is set before sleep, when the count value is equal to the timer value, the system will wake up.

8.2 Registers

LSECRL timer data register

F694H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LSECRL	LSED7	LSED6	LSED5	LSED4	LSED3	LSED2	LSED1	LSED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit7~Bit0 LSED<7:0>: LSE timing/wake-up time data lower 8 bits.

LSECRH timer data register

F695H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LSECRH	LSED15	LSED14	LSED13	LSED12	LSED11	LSED10	LSED9	LSED8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit7~Bit0 LSED<15:8>: LSE timing/wake-up time data higher 8 bits.

LSECON Timer Control Register

F696H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LSECON	LSEEN	LSEWUEN	LSECNTEN	LSESTA	LSEIE	--	--	LSEIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7	LSEEN	LSE module enable control;
	1=	Enable;
	0=	Disable.
Bit6	LSEWUEN	LSE timer wake-up enable control;
	1=	Enable;
	0=	Disable.
Bit5	LSECNTEN	LSE is used for timer counting enable control;
	1=	Enable;
	0=	Disable.
Bit4	LSESTA	LSE stable status bit, read-only;
	1=	LSE is stable;
	0=	LSE is not stable.
Bit3	LSEIE	LSE is used as timer interrupt enable control;
	1=	Enable;
	0=	Disable.
Bit2~Bit1	--	Reserved.
Bit0	LSEIF	LSE as timer interrupt flag bit (cleared by software);
	1=	Generate interrupt.
	0=	No interrupt is generated or the interrupt is cleared.

8.3 Function Description

To use the LSE timer function, you need to set LSEEN=1 to enable the LSE timer function module, and then wait for the LSE clock stable status bit LSETA=1, and then configure the LSE timing value {LSECRH[7:0], LSECRL[7 :0]}, finally set LSECNT=1, enable LSE counting, and turn on the LSE counting function. The LSE timer starts counting from 0. When the count value is equal to the timing value, the interrupt flag is set to 1, and the timing value is updated to the value in the timer data register (that is, the LSE timing value is the last time before the count value and the timing value are equal Write the value of {LSECRH[7:0], LSECRL[7:0]}). The minimum timer value of the timer is 1. If the timer value is set to 0, the timer defaults to 1 as the timer value. The formula for calculating the timing time of the LSE timer is as follows:

$$\text{LSE timing time} = \frac{1}{32.768} \times (\{\text{LSECRH[7:0]}, \text{LSECRL[7:0]}\}+1)\ \text{ms}$$

If any bit of LSEEN, LSECNTEN, LSETA is 0, the count value of LSE will be cleared.

8.4 Interrupt and Sleep Wakeup

When the count value of the LSE timer is equal to the timing value, the timer interrupt flag bit LSEIF is set to 1. If the global interrupt is enabled (EA=1) and the LSE timer interrupt is enabled (LSEIE=1), the CPU will execute the interrupt service routine.

To use LSE timer interrupt to wake up the sleep mode, you need to turn on LSEEN, LSECNT, LSEWIEN before sleep, and set the time from sleep state to wakeup{LSECRH[7:0],LSECRL[7:0]}. If the global interrupt enable and LSE interrupt enable are turned on before the sleep, after the sleep wakes up, the interrupt service routine will be executed first, and the next instruction of the sleep instruction will be executed after the interrupt returns.

9. Timer0/1

Timer 0 is similar in type and structure to Timer 1, and is two 16-bit timers. Timer 1 has three working modes, and Timer 0 has four working modes. They provide basic timing and event counting operations.

- In the "timer mode", the timer register is incremented every 12 or 4 system cycles when the timer clock is enabled.
- In the "counter mode", the timing register will increase whenever it detects a falling edge on the corresponding input pin (T0 or T1).

9.1 Overview

Timer 0 and Timer 1 are fully compatible with standard 8051 timers.

Each timer consists of two 8-bit registers: {TH0 (0x8C): TL0 (0x8A)} and {TH1 (0x8D): TL1 (0x8B)}. Timers 0 and 1 work in four identical modes. Timer0 and Timer1 modes are described below.

Mode	M1	M0	Function description
0	0	0	THx[7:0], TLx[4:0] form a 13-bit timer/counter
1	0	1	THx[7:0], TLx[7:0] form a 16-bit timer/counter
2	1	0	TLx[7:0] form 8-bit automatic reload timer/counter, reload from THx
3	1	1	TL0, TH0 are two 8-bit timer/counters, Timer1 stop counting

Register THx and TLx are special function registers, it has the function of storing the actual timer value. THx and TLx can be cascaded into 13-bit or 16-bit registers through mode options. Each time an internal clock pulse is received or a state transition occurs on the external timer pin, the value of the register is increased by one. The timer will start counting from the value loaded in the preset register until the timer overflows, at which time an internal interrupt signal will be generated. If the automatic reload mode of the timer is selected, the timer value will be reset to the initial value of the preload register and continue counting, otherwise the timer value will be reset to zero. Note that in order to get the maximum calculation range of the timer/counter, the preset register must be cleared first.

9.2 Timer0/1 Registers

9.2.1 Timer0/1 Mode Register (TMOD)

0x89	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMOD	GATE1	CT1	T1M1	T1M0	GATE0	CT0	T0M1	T0M0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 GATE1: Timer 1 gate control bit;
1= Enable;
0= Disable.

Bit6 CT1: Timer 1 timing/counting selection bit;
1= Counting;
0= Timing.

Bit5~ Bit4 T1M1, T1M0: Timer 1 mode selection bit;
00= Mode 0, 13-bit timer/counter;
01= Mode 1, 16-bit timer/counter;
10= Mode 2, 8-bit automatic reload timing /Counter;
11= Mode 3, stop counting.

Bit3 GATE0: Timer 0 gate control bit;
1= Enable;
0= Disable.

Bit2 CT0: Timer 0 timing/counting selection bit;
1= Counting;
0= Timing.

Bit1~ Bit0 T0M1, T0M0: Timer 0 mode selection bits;
00= Mode 0, 13-bit timer/counter;
01= Mode 1, 16-bit timer/counter;
10= Mode 2, 8-bit automatic reload timing /Counter;
11= mode 3, two independent 8-bit timers/counters.

9.2.2 Timer0/1 Control Register (TCON), Bit-Addressable.

0x88	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 TF1: Timer1 counter overflow interrupt flag bit;
1= Timer1 counter overflows and enters the interrupt service routine. The hardware is automatically cleared;
0= Timer1 counter does not overflow.
Bit6 TR1: Timer1 running control bit;
1= Timer1 is started;
0= Timer1 is closed.
Bit5 TF0: Timer0 counter overflow interrupt flag bit;
1= Timer0, and the hardware is automatically cleared when entering the interrupt service routine;
0= Timer0 counter does not overflow.
Bit4 TR0: Timer0 running control bit;
1= Timer0 is started;
0= Timer0 is closed.
Bit3 IE1: External interrupt 1 flag bit;
1= External interrupt 1 generates an interrupt, and the hardware is automatically cleared when entering the interrupt service routine;
0= External interrupt 1 does not generate an interrupt.
Bit2 IT1: External interrupt 1 trigger mode control bit;
1= falling edge trigger;
0= low level trigger.
Bit1 IE0: External interrupt 0 flag bit;
1= External interrupt 0 generates an interrupt, and the hardware is automatically cleared when entering the interrupt service routine;
0= External interrupt 0 does not generate an interrupt.
Bit0 IT0: External interrupt 0 trigger mode control bit;
1= Falling edge trigger;
0= Low level trigger.

9.2.3 Timer0 Data Register Low (TL0)

0x8A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL0	TL07	TL06	TL05	TL04	TL03	TL02	TL01	TL00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit0 TL07-TL00: Timer 0 low bit data register (also used as counter low bit).

9.2.4 Timer0 Data Register High Bit (TH0)

0x8C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TH0	TH07	TH06	TH05	TH04	TH03	TH02	TH01	TH00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 TH07-TH00: Timer 0 high data register (also used as counter high).

9.2.5 Timer1 Data Register Low (TL1)

0x8B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL1	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 TL17-TL10: Timer 1 low bit data register (also used as counter low bit).

9.2.6 Timer1 Data Register High (TH1)

0x8D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TH1	TH17	TH16	TH15	TH14	TH13	TH12	TH11	TH10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 TH17-TH10: Timer 1 high data register (also used as counter high bit).

9.2.7 Function Clock Control Register (CKCON)

0x8E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CKCON	WTS2	WTS1	WTS0	T1M	T0M	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	1	1	1

Bit7~Bit5 WTS2-WTS0: WDT overflow time selection bit;
000= 2^{17}*Tsys;
001= 2^{18}*Tsys;
010= 2^{19}*Tsys;
011= 2^{20}*Tsys;
100= 2^{21}*Tsys
101= 2^{22}*Tsys;
110= 2^{24}*Tsys;
111= 2^{26}*Tsys.
Bit4 T1M: Timer1 clock source selection bit;
0= Fsys/12;
1= Fsys/4.
Bit3 T0M: Timer0 clock source selection bit;
0= Fsys/12;
1= Fsys/4.
Bit2~Bit0 Not used.

9.3 Timer0/1 Interrupt

Timer0/1 can be enabled or disabled through the IE register, and the high/low priority can also be set through the IP register. The interrupt related bits are as follows:

Interrupt mask register IE (0xA8)

0xA8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 EA: Overall interrupt enable Bit;
1= Enable all interrupts that are not masked;
0= Disable all interrupts.

Bit6 ES1: UART1 interrupt enable bit;
1= Enable UART1 interrupt;
0= Disable UART1 interrupt.

Bit5 ET2: TIMER2 total interrupt enable bit;
1= Enable all TIMER2 interrupts;
0= Disable all TIMER2 interrupts.

Bit4 ES0: UART0 interrupt enable bit;
1= Enable UART0 interrupt;
0= Disable UART0 interrupt.

Bit3 ET1: TIMER1 interrupt enable bit;
1= Enable TIMER1 interrupt;
0= Disable TIMER1 interrupt.

Bit2 EX1: External interrupt 1 interrupt enable bit;
1= Enable external interrupt 1 interrupt;
0= Disable external interrupt 1 interrupt.

Bit1 ET0: TIMER0 interrupt enable bit;
1= Enable TIMER0 interrupt;
0= Disable TIMER0 interrupt.

Bit0 EX0: External interrupt 0 interrupt enable bit;
1= Enable external interrupt 0 interrupt;
0= Disable external interrupt 0 interrupt.

Interrupt Priority Control Register IP

0xB8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IP	--	PS1	PT2	PS0	PT1	PX1	PT0	PX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 --

Bit6 PS1: UART1 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit5 PT2: TIMER2 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit4 PS0: UART0 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit3 PT1: TIMER1 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit2 PX1: External interrupt 1 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit1 PT0: TIMER0 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit0 PX0: External interrupt 0 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Timer0/1, INT0/1 Interrupt Flag Register (TCON), Bit-Addressable.

0x88	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 TF1: Timer1 counter overflow interrupt flag bit;
1= Timer1 counter overflows, automatically cleared by hardware when entering the interrupt service routine, or cleared by software;
0= Timer1 counter does not overflow.
Bit6 TR1: Timer1 running control bit;
1= Timer1 is started;
0= Timer1 is closed.
Bit5 TF0: Timer0 counter overflow interrupt flag bit;
1= Timer0 counter overflows, it is automatically cleared by hardware when entering the interrupt service routine, or can be cleared by software;
0= Timer0 counter has no overflow.
Bit4 TR0: Timer0 running control bit;
1= Timer0 is started;
0= Timer0 is closed.
Bit3 IE1: External Interrupt 1 flag;
1= External Interrupt 1 generates an interrupt, which is automatically cleared by hardware when entering the interrupt service routine, or cleared by software;
0= External Interrupt 1 does not generate an interrupt.
Bit2 IT1: External interrupt 1 trigger mode control bit;
1= Falling edge trigger;
0= Low level trigger.
Bit1 IE0: External interrupt 0 flag bit;
1= External interrupt 0 generates an interrupt, which is automatically cleared by hardware when entering the interrupt service routine, or it can be cleared by software;
0= External interrupt 0 does not generate an interrupt.
Bit0 IT0: External interrupt 0 trigger mode control bit;
1= Falling edge trigger;
0= Low level trigger.

The flag bit that generates an interrupt can be cleared by software, and the result is the same as cleared by hardware. In other words, you can generate interrupts by software (it is not recommended to generate interrupts by writing flag bits) or cancel pending interrupts.

The TF0 and TF1 flags can be cleared by writing 0 when the interrupt is not enabled.

9.4 Timer0 Working Mode

9.4.1 T0 - Mode 0 (13-bit timer/counting mode)

In this mode, Timer0 is a 13-bit register. When all the bits of the counter are turned from 1 to 0, the timer 0 interrupt flag TF0 is set to 1. When TCON.4=1 and TMOD.3=0 or TCON.4=1, TMOD.3=1, T0G=1, the counting input is enabled to timer 0. (Set TMOD.3=1 to allow timer 0 to be controlled by external pin T0G for pulse width measurement). The 13-bit register consists of the lower 5 bits of TH0 and TL0. The upper 3 bits of TL0 should be ignored.

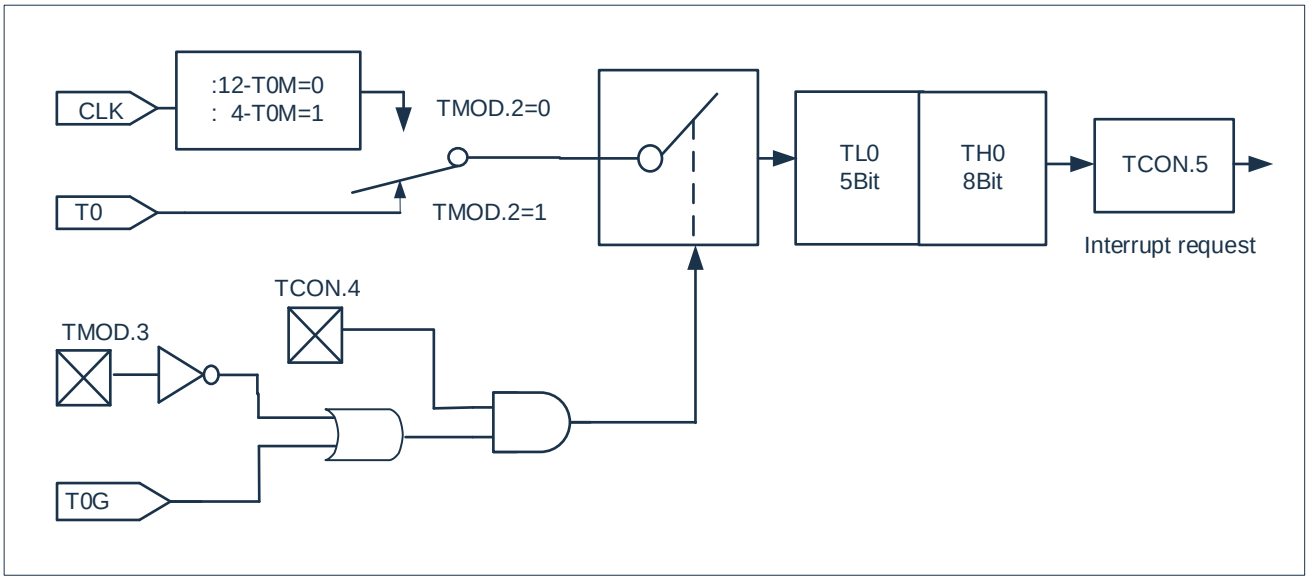


Figure 9-1: Timer0, Mode 0: 13-bit Timer/Counter

9.4.2 T0 - Mode 1 (16-bit timer/counting mode)

Mode 1 is the same as mode 0, except that all 16 bits of the timer 0 data register run in mode 1. Mode 1 block diagram as shown below:

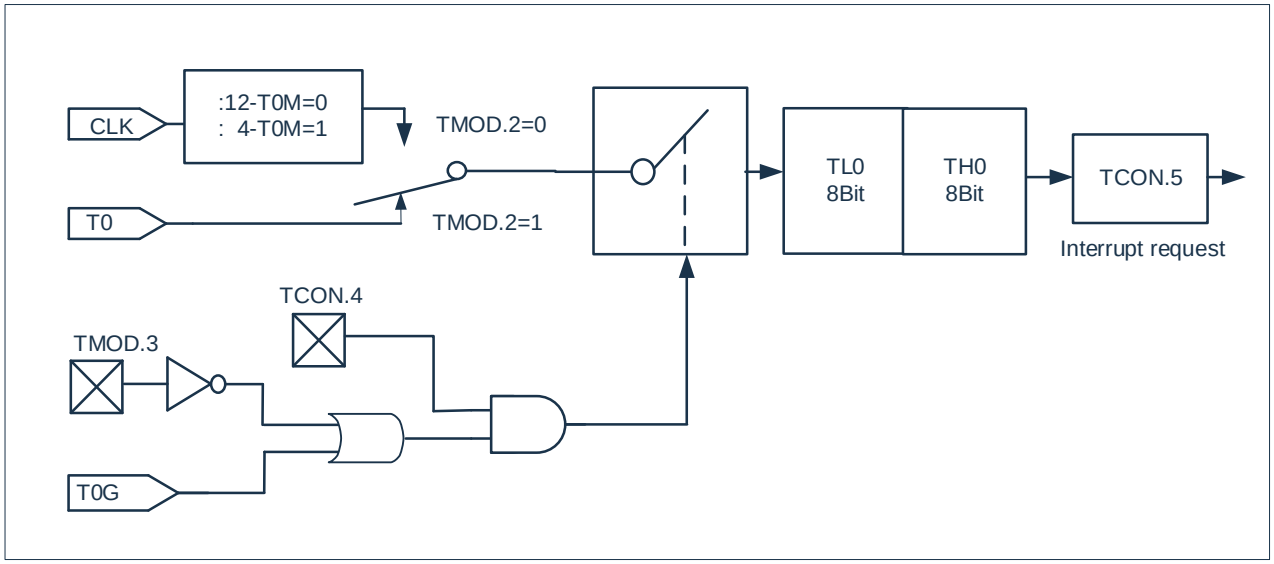


Figure 9-2: Timer0, Mode 1: 16-bit Timer/Counter

9.4.3 T0 - Mode 2 (8-bit auto reload timer/counter mode)

The timer register in mode 2 is an 8-bit counter (TL0) with auto-reload mode, as shown in the figure below. The overflow from TL0 not only sets TF0 to 1, but also reloads the contents of TH0 to TL0 by software. The value of TH0 remains unchanged during the reinstallation process.

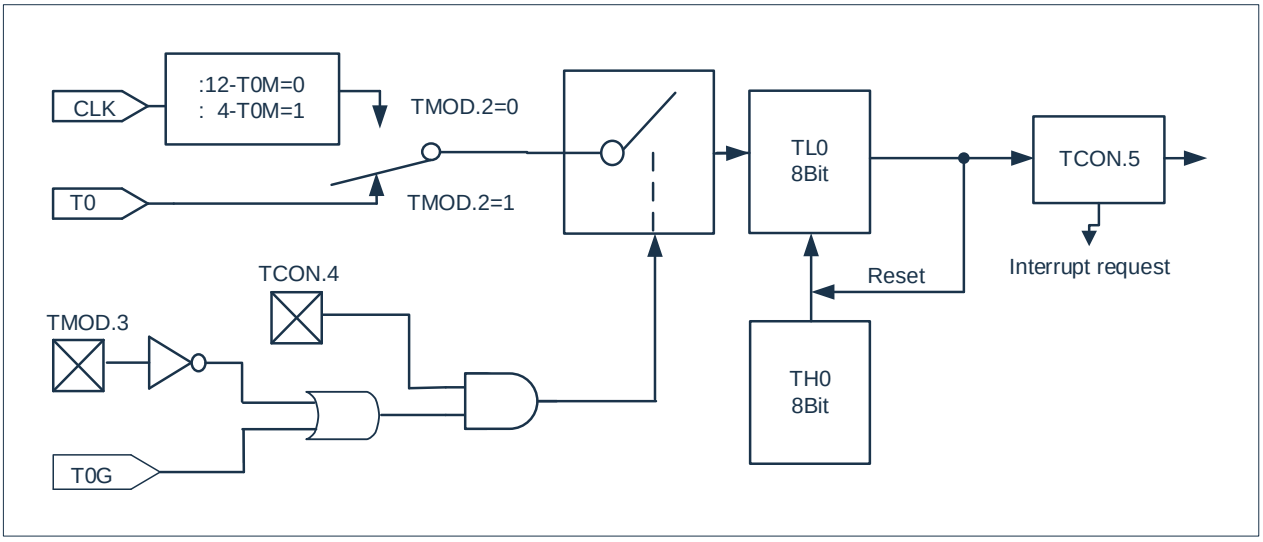


Figure 9-3: Timer0, Mode 2: 8-bit Timer/Counter (Auto Reload)

9.4.4 T0 - Mode 3 (two separate 8-bit timers/counters)

Timer 0 in Mode 3 sets TL0 and TH0 as two independent counters. The logic of Timer 0 Mode 3 is shown in the figure below.

TL0 can work as a timer or counter, and use timer 0 control bits: such as CT0, TR0, GATE0, and TF0.

TH0 can only work as a timer, and uses the TR1 and TF1 flags of timer 1 and controls the interrupt of timer 1.

Mode 3 can be used when two 8-bit timers/counters are required. When timer 0 is in mode 3, timer 1 can be turned off by switching to its own mode 3, or it can still be used as a baud rate generator by the serial channel, or in any case that does not require timer 1 interrupts. In application.

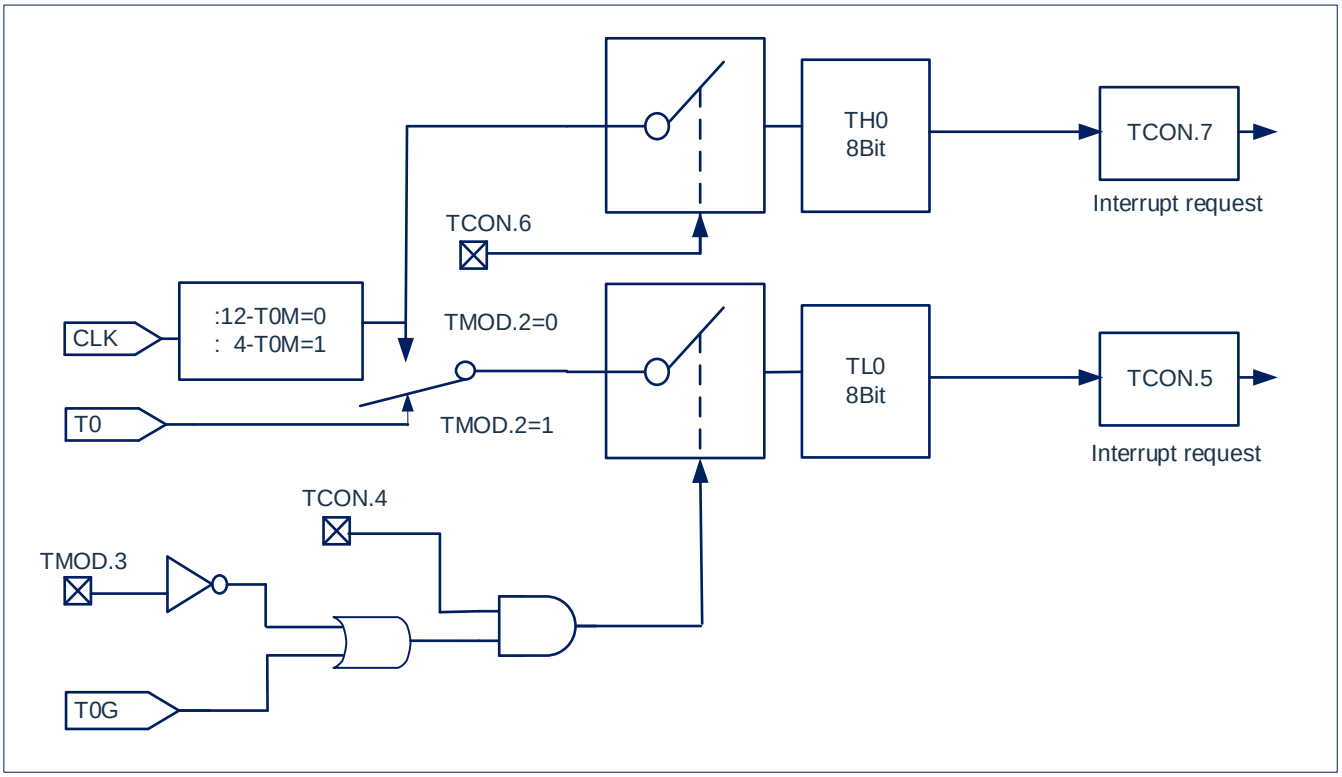


Figure 9-4: Timer0, Mode 3: Two 8-bit Timer/Counter

9.5 Timer1 Working Mode

9.5.1 T1 - Mode 0 (13-bit timer/counting mode)

In this mode, Timer 1 is a 13-bit register. When all the bits of the counter are turned from 1 to 0, the timer 1 interrupt flag TF1 is set to 1. When TCON.6=1 and TMOD.7=0 or when TCON.6=1, TMOD.7=1 and T1G=1, the counting input is enabled to timer 1. (Setting TMOD.7=1 allows Timer 1 to be controlled by the external pin T1G for pulse width measurement). The 13-bit register consists of 8 bits of TH1 and the lower 5 bits of TL1. The upper three bits of TL1 should be ignored. The structure diagram of Timer1 mode 0 is shown in the figure below:

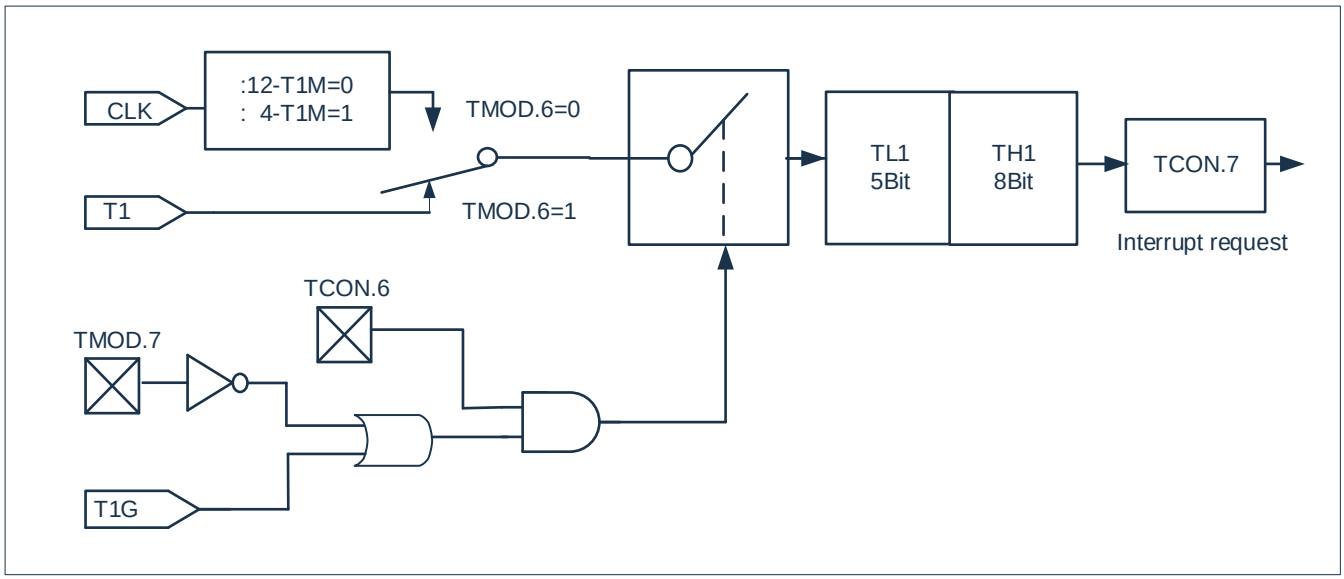


Figure 9-5: Timer1, Mode 0: 13-bit Timer/Counter

9.5.2 T1 - Mode 1 (16-bit timer/counting mode)

Mode 1 is the same as mode 0, except that all 16 bits of the timer 1 register are running in mode 1. The block diagram of Timer1 mode 1 is shown in the figure below:

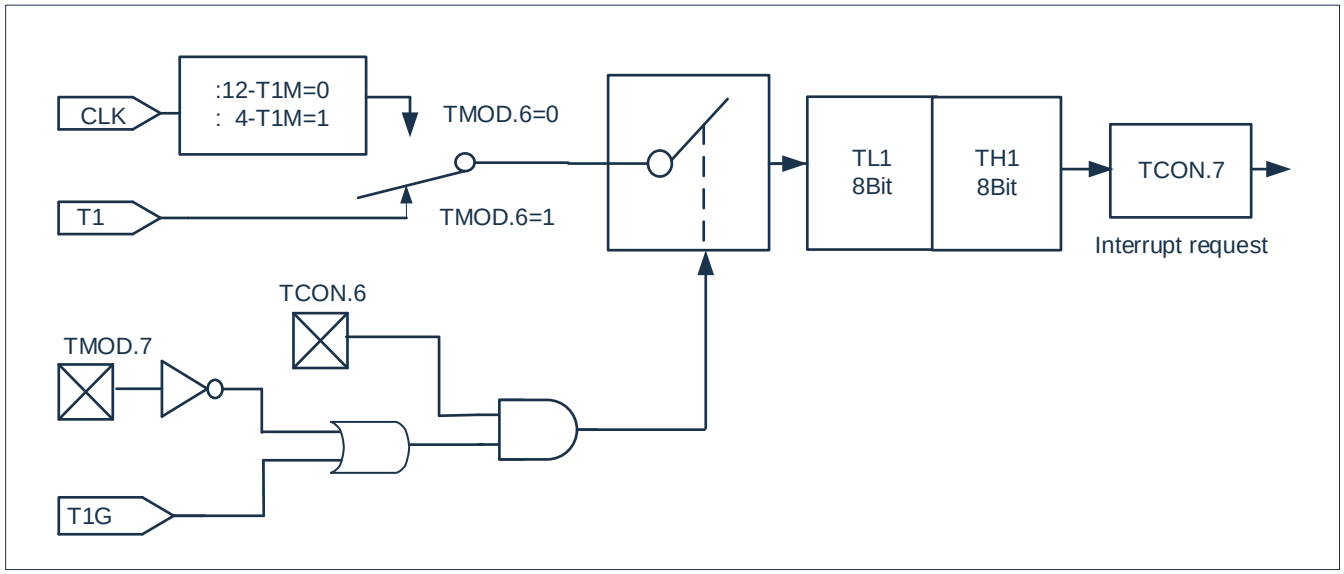


Figure 9-6: Timer1, Mode 1: 16-bit Timer/Counter

9.5.3 T1 - Mode 2 (8-bit auto-reload timer/counting mode)

The timer 1 register in mode 2 is an 8-bit counter (TL1) with auto-reload mode, as shown in the figure below. The overflow from TL1 not only sets TF1 to 1, but also reloads the contents of TH1 to TL1 by software. The value of TH1 remains unchanged during the reinstallation process.

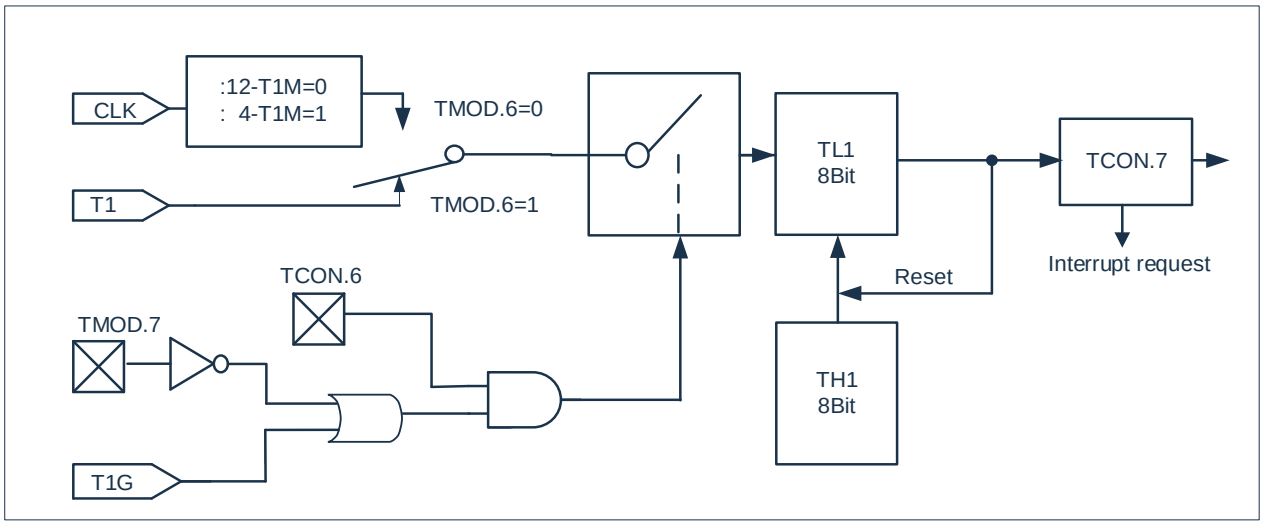


Figure 9-7: Timer1, Mode 2: 8-bit Timer/Counter (Auto Reload)

9.5.4 T1 - Mode 3 (stop counting)

Timer 1 in mode 3 stops counting, and its effect is the same as setting TR1=0.

10. TIMER2

Timer 2 with additional compare/capture/reload functions is one of the core peripheral units. It can be used for various digital signal generation and event capture, such as pulse generation, pulse width modulation, pulse width measurement, etc.

10.1 Overview

The following block diagram shows the general configuration of Timer 2 with additional compare/capture/reload register functionality.

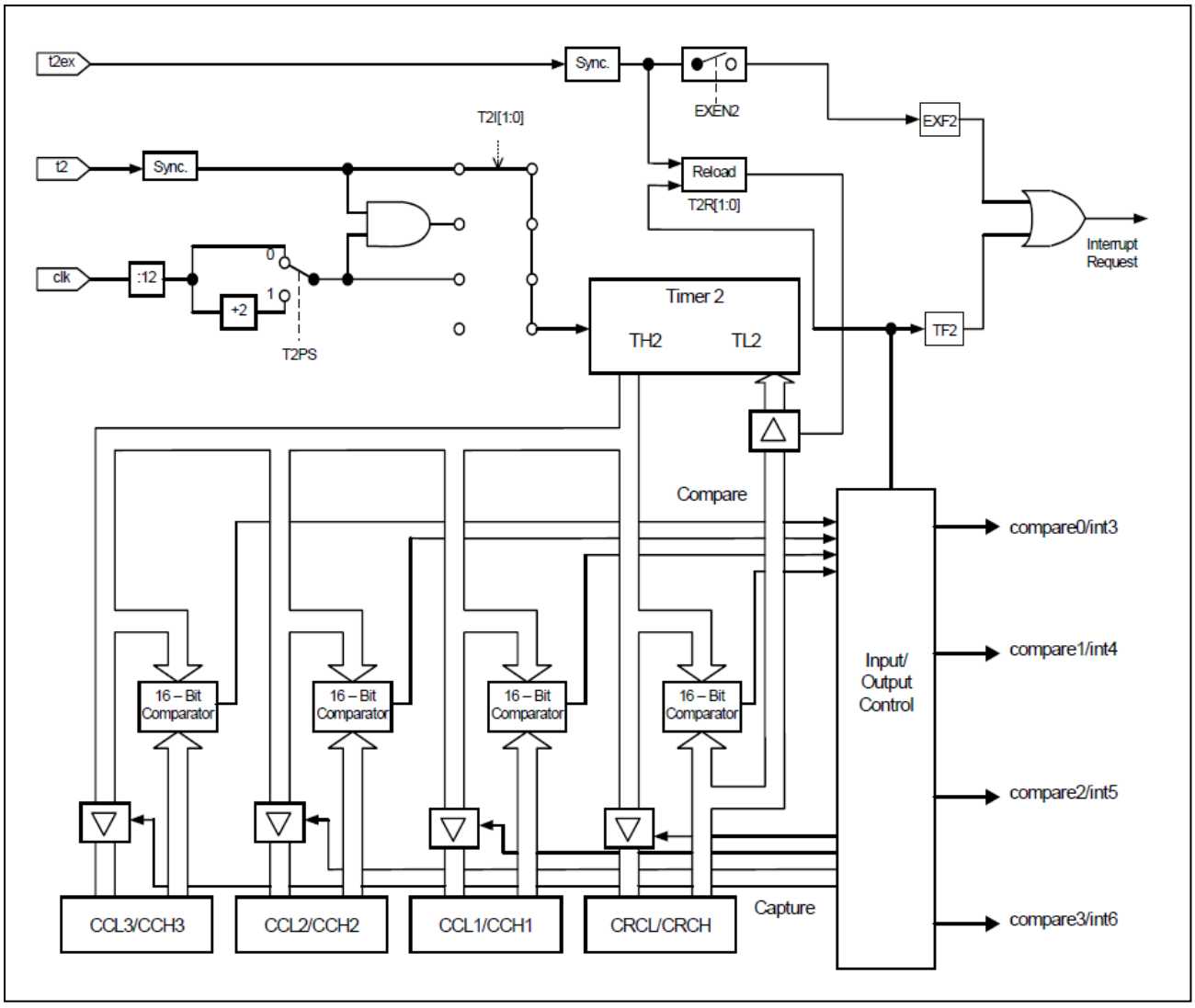


Figure 10-1: Compare/capture module

10.2 Timer2 Registers

The registers of Timer 2 with compare/capture register function are as follows.

10.2.1 T2 Control Register (T2CON)

0xC8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	T2PS	I3FR	CAPES	T2R1	T2R0	T2CM	T2I1	T2I0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7	T2PS:	Timer2 clock prescaler selection bit;
	1=	Fsys/24 ;
	0=	Fsys/12.
Bit6	I3FR:	Capture channel 0 input single edge selection and compare interrupt time selection bit;
		capture channel 0 mode:
	1=	Capture rising edge to RLDL/RLDH register;
	0=	Capture falling edge to RLDL/RLDH register.
		Compare channel 0 mode:
	1=	Interrupt generated when TL2/TH2 and RLDL/RLDH are not equal to equal to each other;interrupt generated when
	0=	TL2/TH2 and RLDL/RLDH are equal to not equal to each other;
Bit5	CAPES:	Capture channel 1-3 input Single edge selection (valid for capture channels 1-3 together).
	0=	Rising edge is captured to the CCL1/CCH1-CCL3/CCH3 register;
	1=	Falling edge is captured to the CCL1/CCH1-CCL3/CCH3 register.
Bit4~Bit3	T2R1-T2R0:	Timer2 loading mode selection bit;
	0x=	Reloading prohibited;
	10=	Loading mode 1: automatic reloading when Timer2 overflows;
	11=	Loading mode 2: reloading on the falling edge of T2EX pin.
Bit2	T2CM:	Compare mode selection;
	1=	Compare mode 1;
	0=	Compare mode 0.
Bit1~ Bit0	T2I1-T2I0:	Timer2 clock input selection bit;
	00=	Timer2 stop;
	01=	System clock frequency division (selected by T2PS control frequency division);
	10=	External pin T2 as event input (event counting mode);
	11=	External pin T2 is used as gate control input (gate timing mode).

10.2.2 Timer2 Data Register Low Bit (TL2)

0xCC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL2	TL27	TL26	TL25	TL24	TL23	TL22	TL21	TL20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 TL27-TL20: Timer 2 low bit data register (also used as counter low bit).

10.2.3 Timer2 Data Register High Bit (TH2)

0xCD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TH2	TH27	TH26	TH25	TH24	TH23	TH22	TH21	TH20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 TH27-TH20: Timer 2 high data register (also used as counter low).

10.2.4 Timer2 Compare/Capture/Auto-Reload Register Low Bit (RLDL)

0xCA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RLDL	RLDL7	RLDL6	RLDL5	RLDL4	RLDL3	RLDL2	RLDL1	RLDL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 RLDL7- RLDL0: Timer 2 compare/capture/auto-reload register low bit.

10.2.5 Timer2 Compare/Capture/Auto-Reload Register High Bit (RLDH)

0xCB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RLDH	RLDH7	RLDH6	RLDH5	RLDH4	RLDH3	RLDH2	RLDH1	RLDH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 RLDH7- RLDH0: Timer 2 compare/capture/auto-reload register high bit.

10.2.6 Timer2 Compare/Capture Channel 1 Register Low Bit (CCL1)

0xC2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CCL1	CCL17	CCL16	CCL15	CCL14	CCL13	CCL12	CCL11	CCL10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 CCL17-CCL10: Timer 2 compare/capture channel 1 register low bit.

10.2.7 Timer2 Compare/Capture Channel 1 Register high Bit (CCH1)

0xC3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CCH1	CCH17	CCH16	CCH15	CCH14	CCH13	CCH12	CCH11	CCH10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 CCH17-CCH10: Timer 2 compare/capture channel 1 register high bit.

10.2.8 Timer2 Compare/Capture Channel 2 Register Low Bit (CCL2)

0xC4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CCL2	CCL27	CCL26	CCL25	CCL24	CCL23	CCL22	CCL21	CCL20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 CCL27-CCL20: Timer 2 compare/capture channel 2 register low bit.

10.2.9 Timer2 Compare/Capture Channel 2 Register High Bit (CCH2)

0xC5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CCH2	CCH27	CCH26	CCH25	CCH24	CCH23	CCH22	CCH21	CCH20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 CCH27-CCH20: Timer 2 compare/capture channel 2 register high bit.

10.2.10 Timer2 Compare/Capture Channel 3 Register Low Bit (CCL3)

0xC6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CCL3	CCL37	CCL36	CCL35	CCL34	CCL33	CCL32	CCL31	CCL30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 CCL37-CCL30: Timer 2 compare/capture channel 3 register low bit.

10.2.11 Timer2 Compare/Capture Channel 3 Register High Bit (CCH3)

0xC7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CCH3	CCH37	CCH36	CCH35	CCH34	CCH33	CCH32	CCH31	CCH30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 CCH37-CCH30: Timer 2 compare/capture channel 3 register high bit.

10.2.12 T2 Compare Capture Control Register (CCEN)

0xCE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CCEN	CMH3	CML3	CMH2	CML2	CMH1	CML1	CMH0	CML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 CMH3-CML3: Capture/compare mode control bit;
- 00= Capture/compare prohibited;
- 01= Capture operation is triggered on the rising or falling edge of channel 3 (CAPES selection) ;
- 10= Compare mode enable;
- 11= Capture operation is triggered when writing CCL3 or the double-edge trigger of channel 3.

Bit5~Bit4 CMH2-CML2: Capture/compare mode control bit;
- 00= Capture/comparison disabled;
- 01= Capture operation is triggered on the rising or falling edge of channel 2 (CAPES selection);
- 10= Compare mode enable;
- 11= Capture The operation is triggered when writing CCL2 or the double-edge trigger of channel 2.

Bit3~Bit2 CMH1-CML1: Capture/compare mode control bit;
- 00= Capture/compare disabled;
- 01= Capture operation is triggered on the rising or falling edge of channel 1 (CAPES selection);
- 10= Comparison mode enable;
- 11= Capture The operation is triggered when writing CCL1 or the double-edge trigger of channel 1.

Bit1~Bit0 CMH0-CML0: Capture/compare mode control bit;
- 00= Capture/comparison disabled;
- 01= Capture operation is triggered on the rising or falling edge of channel 0 (I3FR selection);
- 10= Comparison mode enable;
- 11= Capture The operation is triggered when RLDL is written or the double edge of channel 0 is triggered.

10.3 Timer2 Interrupt

Timer 2 can enable or disable interrupts through the IE register, and can set high/low priority through the IP register:

Interrupt Mask Register IE (0xA8)

0xA8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 EA: Overall interrupt enable bit;
1= Enable all unmasked interrupts;
0= Disable all interrupts.
Bit6 ES1: UART1 interrupt enable bit;
1= Enable UART1 interrupt;
0= Disable UART1 interrupt.
Bit5 ET2: TIMER2 total interrupt enable bit;
1= Enable all TIMER2 interrupts;
0= Disable all TIMER2 interrupts.
Bit4 ES0: UART0 interrupt enable bit;
1= Enable UART0 interrupt;
0= Disable UART0 interrupt.
Bit3 ET1: TIMER1 interrupt enable bit;
1= Enable TIMER1 interrupt;
0= Disable TIMER1 interrupt.
Bit2 EX1: External interrupt 1 interrupt enable bit;
1= Enable external interrupt 1 interrupt;
0= Disable external interrupt 1 interrupt.
Bit1 ET0: TIMER0 interrupt enable bit;
1= Enable TIMER0 interrupt;
0= Disable TIMER0 interrupt.
Bit0 EX0: External interrupt 0 interrupt enable bit;
1= Enable external interrupt 0 interrupt;
0= Disable external interrupt 0 interrupt.

Interrupt priority control register (IP)

0xB8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IP	--	PS1	PT2	PS0	PT1	PX1	PT0	PX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 --

Bit6 PS1: UART1 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit5 PT2: TIMER2 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit4 PS0: UART0 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit3 PT1: TIMER1 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit2 PX1: External interrupt 1 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit1 PT0: TIMER0 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Bit0 PX0: External interrupt 0 interrupt priority control bit;
1= Set as advanced interrupt;
0= Set as low-level interrupt.

Timer2 Interrupt Mask Register T2IE

0xCF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2IE	T2OVIE	T2EXIE	--	--	T2C3IE	T2C2IE	T2C1IE	T2C0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 T2OVIE: Timer2 overflow interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit6 T2EXIE: Timer2 external load interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit5~Bit4 --
Bit3 T2C3IE: Timer2 compare channel 3 interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit2 T2C2IE: Timer2 compare channel 2 interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit1 T2C1IE: Timer2 compare channel 1 interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.
Bit0 T2C0IE: Timer2 compare channel 0 interrupt enable bit;
1= Enable interrupt;
0= Disable interrupt.

If turn on the interrupt of Timer2, you also need to turn on the total interrupt enable bit ET2=1 (IE.5=1) of Timer2.

Timer2 Interrupt Flag Register T2IF (0xC9)

0xC9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2IF	TF2	T2EXIF	--	--	T2C3IF	T2C2IF	T2C1IF	T2C0IF
R/W	R/W	R/W	--	--	R/W	R/W	R/W	R/W
Reset value	0	0	--	--	0	0	0	0

Bit7 TF2: Timer2 counter overflow interrupt flag bit;
1= Timer2 counter overflows and needs to be cleared by software;
0= Timer2 counter does not overflow.
Bit6 T2EXIF: Timer2 external load flag bit;
1= Timer2 T2EX port generates a falling edge, which needs to be cleared by software;
0= -
Bit5 --
Bit4 --
Bit3 T2C3IF: Timer2 compare/capture channel 3 flag bit;
1= Timer2 compare channel 3 {CCH3:CCL3}={TH2:TL2} or capture channel 3 has a capture operation, which needs to be cleared by software.
0= -
Bit2 T2C2IF: Timer2 compare/capture channel 2 flag bit;
1= Timer2 compare channel 2 {CCH2:CCL2}={TH2:TL2} or capture channel 2 has a capture operation, which needs to be cleared by software.
0= -
Bit1 T2C1IF: Timer2 compare/capture channel 1 flag bit;
1= Timer2 compare channel 1 {CCH1:CCL1}={TH2:TL2} or capture channel 1 has a capture operation, which needs to be cleared by software.
0= -
Bit0 T2C0IF: Timer2 compare/capture channel 0 flag bit;
1= Timer2 compare channel 0{RLDH:RLDL}={TH2:TL2} or capture channel 0 has a capture operation, which needs to be cleared by software.
0= -

10.3.1 Timer Interrupt

When the Timer2 timer overflows, an interrupt is generated. TF2 flag will be set to 1.

10.3.2 External Trigger Interrupt

An interrupt is also generated at falling edge of the T2EX pin, while T2EXIE bit is set. T2EXIF flag will set to 1.

10.3.3 Compare Interrupt

All 4 comparison channels support comparison interrupts.

Compare Channel 0 selects the moment when the compare interrupt is generated, and generating the interrupt sets the compare channel 0 interrupt flag T2C0IF to 1.

I3FR = 0 when TL2/TH2 and RLDL/RLDH generate interrupts from unequal to equal moments;

I3FR = 1 when TL2/TH2 and RLDL/RLDH generate interrupts from equal to unequal moments;

The comparison channels 1-3 cannot select the interrupt generation moment, fixed as TL2/TH2 and CCxL/CCxH generate interrupts from unequal to equal moments. If an interrupt is generated, the interrupt flag T2CxIF of the corresponding comparison channel x is set to 1.

Timer2 all related interrupts share a common interrupt vector, after entering the interrupt service program, you need to judge the related flag bit to determine which situation has generated the interrupt.

10.3.4 Capture Interrupt

All four capture channels support external capture interrupts. When a capture operation is generated, the interrupt flag of the corresponding capture channel is set to T2CxIF.

Note that the write capture method does not generate interrupts.

10.4 Timer2 Function Description

Timer 2 is a 16-bit register that can operate as a timer, event counter or gated timer.

10.4.1 T2 Timing Mode

In timer function, the clock source is derived from system frequency .The prescaler offers the possibility of selecting the 1/12 or 1/24 of system frequency. Thus, the 16-bit timer register (consisted of TH2 and TL2) is either incremented in every 12 clock periods or in every 24 clock periods. The prescaler is selected by bit T2PS of T2CON.

10.4.2 T2 Reload Mode

The reload mode for Timer 2 is selected by the T2R0 and T2R1 bits of T2CON.

In mode 1, When counter 2 is inverted by all 1s to 0 (counter overflow), not only TF2 is set, but timer 2 is registered. The device automatically loads the 16-bit value from the RLDL/RLDH register. The required RLDL/RLDH value can be preset by software. The reload occurs in the same clock cycle as TF2 is set, thus overwriting the count value of 0x0000.

In mode 2, the 16-bit reassembly operation from the RLDL/RLDH register is triggered by the descent edge of the corresponding T2EX input pin. In addition, if T2EXIE=1, the T2EXIF flag will be set to 1. If timer 2 total interrupts enable (ET2=1), an interrupt occurs.

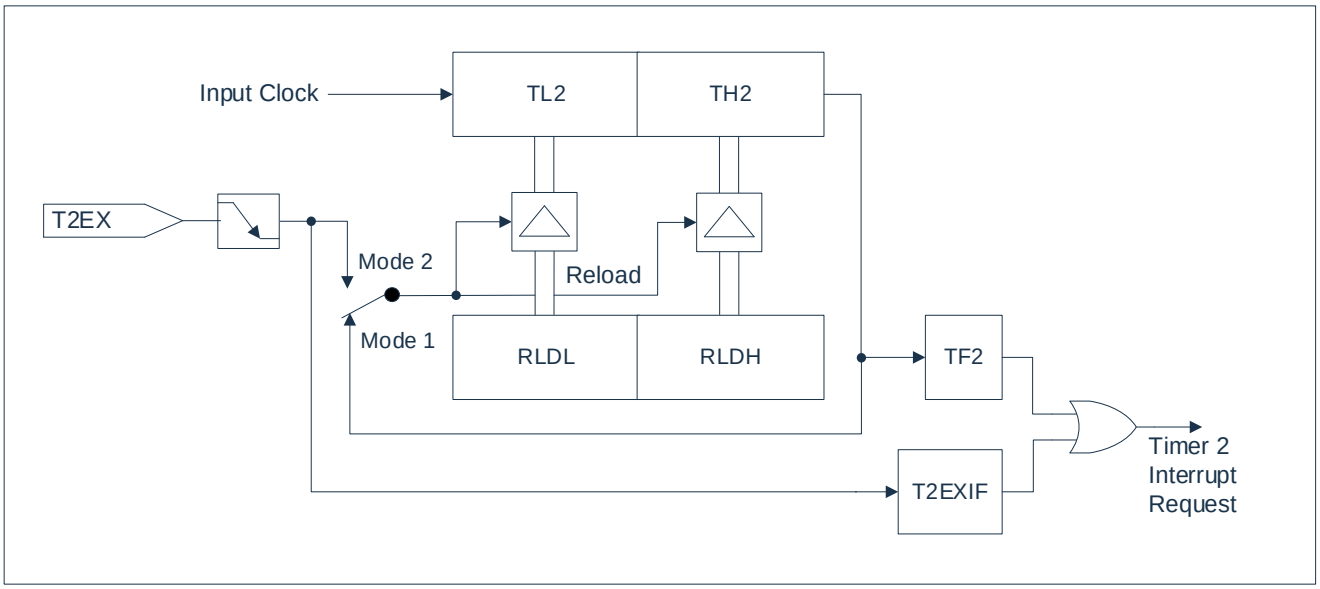


Figure 10-2: Timer2 reload mode block diagram

10.4.3 Timer2 Gate Timing Mode

For gate timer function, the external input pin T2 is used as the input gating for Timer 2. If the T2 pin is high, the internal clock input is selected to the timer, and a low T2 pin terminates the count. This function is often used to measure the pulse width.

10.4.4 Timer2 Event Counting Mode

While in the counter function, Timer 2 is incremented with a 1 to 0 transition on its corresponding external input pin T2. In this function, the external input is sampled at each clock cycle. The count is increased when the sampled input shows high in one cycle and low in the next cycle. The new count value appears in the timer register when the change from high to low on the T2 pin is detected again in the next cycle.

10.5 Compare/PWM Function

The compare function of a timer/register combination can be described as follows:

The 16-bit value stored in a compare/capture register is compared with the contents of the timer register. If the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin, and an interrupt is requested.

Variation of this time stamp somehow changes the wave of a rectangular output signal at a port pin. This may as a variation of the duty cycle of a periodic signal be used for pulse width modulation(PWM) as well as for a continually controlled generation of any kind of square waveforms.

The channel of the compare function output is CC0, CC1, CC2, CC3. Output signals corresponding to the comparison of the {TH2, TL2} registers of the 16-bit compare registers {RLDH, RLDL}, {CCH1, CCL1}, {CCH2, CCL2}, {CCH3, CCL3} and Timer2, respectively.

The compare function consists of two modes: compare modes 0 and 1 are selected by bit T2CM in the special function register T2CON.Two compare modes are implemented to cover a wide range of possible applications.

10.5.1 Compare Mode 0

In mode 0, upon matching the timer and compare register contents, an output signal changes from low to high. It goes back to a low level on timer overflow. Figure below shows a functional diagram of a port register in compare mode 0. The compare output channel is directly controlled by two events: timer overflow and compare operation.

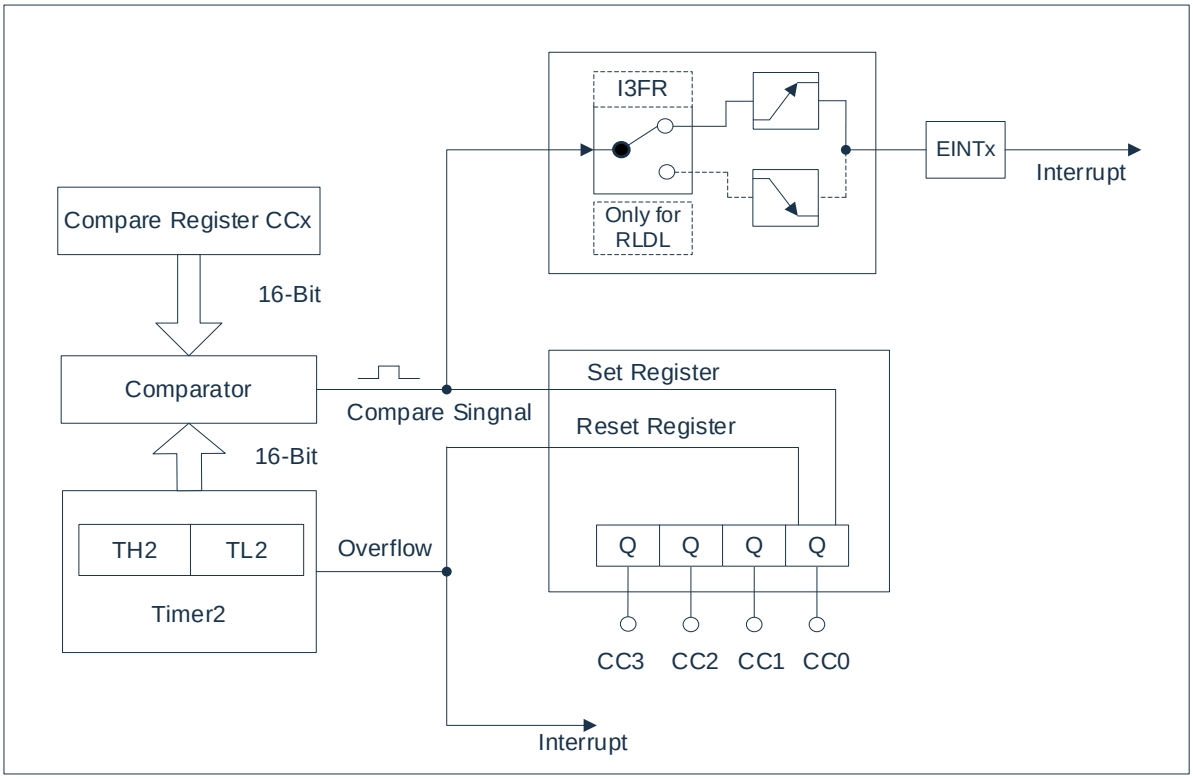


Figure 10-3: Timer2 compare mode 0 block diagram

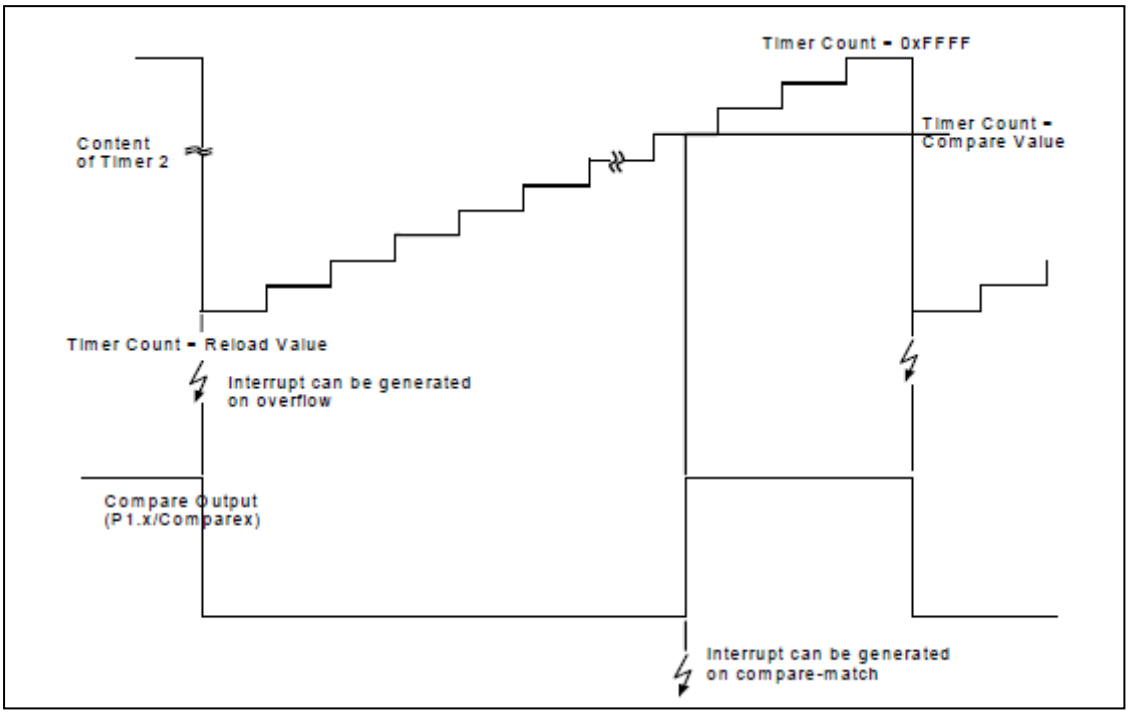


Figure 10-4: Timer 2 compare mode 0 function

10.5.2 Compare Mode 1

In compare mode 1, the software adaptively determines the transition of the output signal. It is commonly used when output signals are not related to a constant signal period. In compare mode 1, both transitions of a signal can be controlled. Compare outputs in this mode can be considered as high speed outputs do not depend on the CPU activity.

If mode 1 is enabled, and the software writes to an appropriate output register of PORT 1, a new value will not appear at the output pin until the next compare match occurs. User can select this way whether the output signal should make a new transition or should keep its old value, until the Timer 2 counter matches the stored compare value. Figure below shows a functional diagram of Timer 2 in compare mode 1.

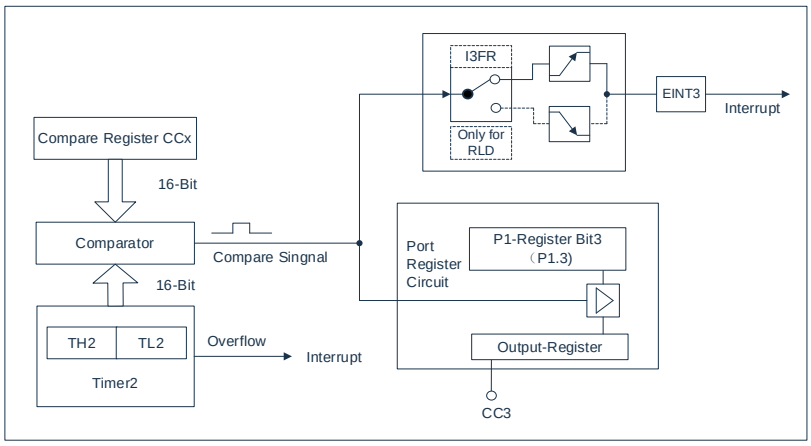


Figure 10-5: Timer 2 compare mode 1 block diagram

Note: Compare mode 1 is only valid for compare channel 3.

10.6 Capture Function

Each of the four 16-bit compare/capture registers {RLDH, RLDL}, {CCH1, CCL1}, {CCH2, CCL2}, {CCH3, CCL3} can be used to latch the current 16-bit value of the Timer 2 registers {TH2, TL2}. Two different modes are provided for this function.

In mode 0, an external event latches Timer 2 contents to a dedicated capture register.

In mode 1, a capture will occur upon writing to the low order byte {RLDL/CCL1/CCL2/CCL3 }of the dedicated 16-bit capture register. This mode is provided to allow software reading of Timer 2 contents {TH2, TL2} on the fly.

Capture channel 0~3 can select any of the input pins CAP0-CAP as the input source signal. The following is the control method for the corresponding capture channel:

Capture channel	Input pin
0	CAP0
1	CAP1
2	CAP2
3	CAP3

10.6.1 Capture Mode 0

The external events that result in capture in this mode are:

- For CC registers 1 to 3: captures positive or negative jumps on channels 1-3, and can also support positive and negative jumps.
- For RLD register: captures positive or negative jumps on channel 0. Positive and negative jumps can also be supported.

Whether the capture on channel 0 is a positive or negative jump trigger capture operation depends on the I3FR bit of T2CON. I3FR=0, negative jump trigger capture; I3FR=1, positive jump trigger capture.

Whether the capture operation on capture channels 1-3 is triggered by positive or negative jumps depends on the CAPES bit of T2CON. The selected jumping method for capture channels 1-3 is the same

In addition, capture channels 0-3 also support double-jump capture operation by selecting the corresponding operating mode control bit of CCEN register as 11. It should be noted that this working mode also supports capture mode 1, i.e. write operation can generate capture action.

All external capture events for channels 0-3 can generate interrupts.

10.6.2 Capture Mode 1

In mode 1 capture occurs in response to a write instruction to the low order byte of a capture register. The write-to register signal (e.g. write to RLDL) is used to initiate a capture. The value written to the dedicated capture register is irrelevant for this function. The timer 2 contents will be latched into the appropriate capture register in the cycle following the write instruction. In this mode, no interrupt request will be generated.

Figures below show functional diagrams of the timer 2 capture function.

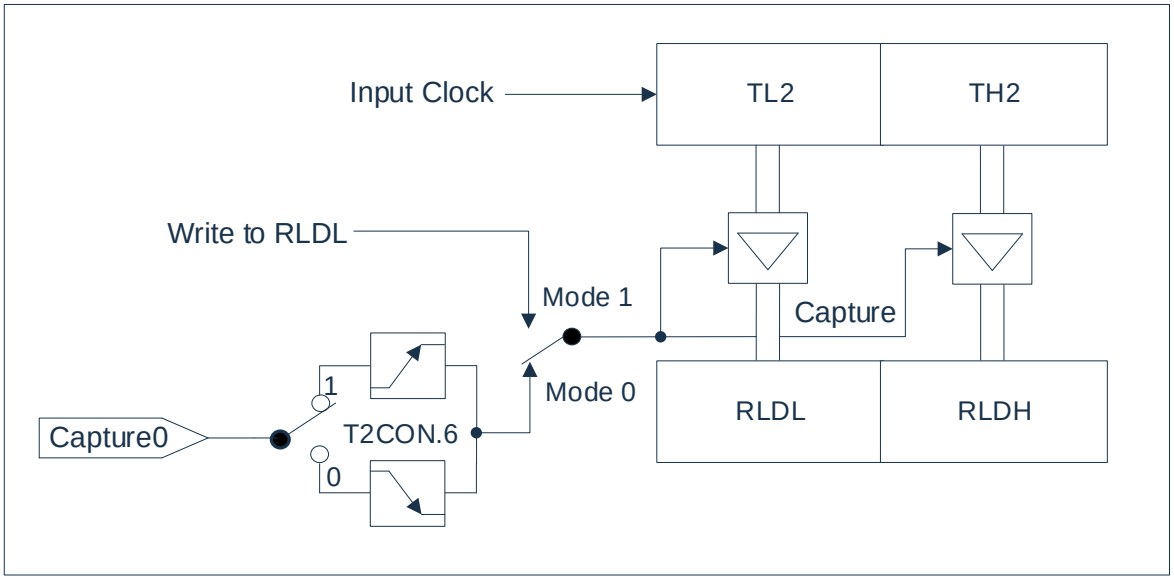


Figure 10-6: Timer 2 capture mode 0 for RLDL and RLDH registers block diagram

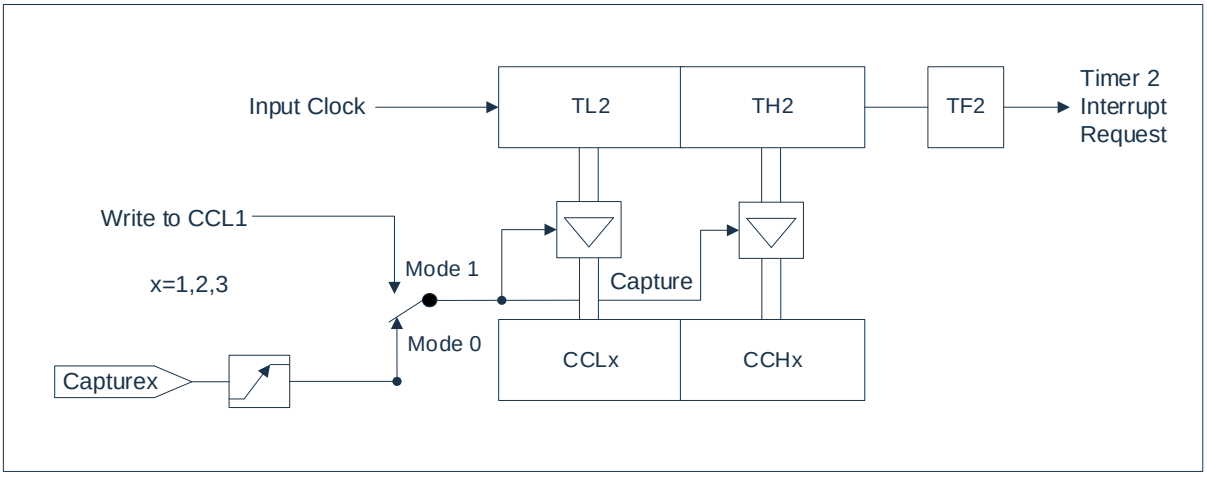


Figure 10-7: Timer 2 capture mode 0 for CCLx and CCHx registers block diagram

11. TIMER3/4

Timer 3/4 are similar to Timer 0/1 and they are two 16-bit timers. Timer 3 has four operating modes, and Timer 4 has three operating modes. Compared with Timer0/1, Timer3/4 only provides timing operations.

The register is incremented in every 12 clock periods or in every 4 clock periods, when timer is enabled.

11.1 Overview

Timer 3 and Timer 4 are composed of two 8-bit registers {TH3, TL3} and {TH4, TL4}, respectively. Timer 3 and 4 are operating in four same modes. The modes of Timer3 and Timer4 are as follows:

Mode	M1	M0	Function description
0	0	0	{THx[7:0], TLx[4:0] }as a 13-bit timer
1	0	1	{THx[7:0], TLx[7:0] } as a 16-bit timer
2	1	0	TLx[7:0] as an 8-bit Auto-Reload timer , reloading from THx
3	1	1	{TL3}, {TH3 } as two separate 8-bit timers, Timer4 stops timing.

11.2 Timer3/4 Register

11.2.1 Timer3/4 Control Register (T34MOD)

0xD2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T34MOD	TR4	T4M	T4M1	T4M0	TR3	T3M	T3M1	T3M0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 TR4: Timer 4 timer enable bit
1= Enable;
0= Disable.
Bit6 T4M: Timer 4 clock selection bit
1= Fsys/4;
0= Fsys/12.
Bit5~Bit4 T4M1, T4M0: Timer 4 mode selection bit
00= Mode 0,13-bit timer;
01= Mode 1,16-bit timer;
10= Mode 2,8-bit Auto-Reload timer;
11= Mode 3,Stop timer.
Bit3 TR3: Timer 3timer enable bit
1= Enable;
0= Disable.
Bit2 T3M: Timer 4 clock selection bit
1= Fsys/4;
0= Fsys/12.
Bit1~Bit0 T3M1, T3M0: Timer 3 mode selection bit
00= Mode 0,13-bit timer;
01= Mode 1, 16-bit timer;
10= Mode 2, 8-bit auto-reload timer;
11= Mode 3, two separate 8-bit timers.

11.2.2 Timer 3 Data Register Lower Bit (TL3)

0xDA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL3	TL37	TL36	TL35	TL34	TL33	TL32	TL31	TL30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 TL37-TL30: Timer 3 Low 8-bit data register (also as lower bit of the timer).

11.2.3 Timer 3 Data Register Higher Bit (TH3)

0xDB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TH3	TH37	TH36	TH35	TH34	TH33	TH32	TH31	TH30
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 TH37-TH30: Timer 3 High 8-bit data register. (also as higher bit of the timer)

11.2.4 Timer 4 Data Register Lower Bit (TL4)

0xE2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL4	TL47	TL46	TL45	TL44	TL43	TL42	TL41	TL40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 TL47-TL40: Timer 4 Low 8-bit data register (also as lower bit of the timer)

11.2.5 Timer 4 Data Register Higher Bit (TH4)

0xE3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TH4	TH47	TH46	TH45	TH44	TH43	TH42	TH41	TH40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 TH47-TH40: Timer 4 High 8-bit data register. (also as higher bit of the timer)

11.3 Timer3/4 Interrupt

Timer 3/4 interrupts can be enabled or disabled by the IE register. The high/low priority can also be set by the IP register. The interrupt related bits are as follows:

Interrupt Mask Register EIE2

0xAA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIE2	SPIIE	I2CIE	WDTIE	ADCIE	PWMIE	--	ET4	ET3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPIIE: SPI Interrupt enable bit
1= Enable SPI interrupt;
0= Disable SPI interrupt.
Bit6 I2CIE I2C Interrupt enable bit
1= Enable I^2C interrupt;
0= Disable I^2C interrupt.
Bit5 WDTIE: WDT Interrupt enable bit
1= Enable WDT interrupt;
0= Disable WDT interrupt.
Bit4 ADCIE: ADC Interrupt enable bit
1= Enable ADC interrupt;
0= Disable ADC interrupt.
Bit3 PWMIE: PWM global interrupt enable bit
1= Enable PWM global interrupt;
0= Disable PWM global interrupt.
Bit2 --
Bit1 ET4: Time4 Interrupt enable bit
1= Enable Time4 interrupt;
0= Disable Time4 interrupt.
Bit0 ET3: Time3 Interrupt enable bit
1= Enable Time3 interrupt;
0= Disable Time3 interrupt.

Peripheral Interrupt Status Register EIF2 (0xB2)

0xB2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIF2	SPIIF	I2CIF	--	ADCIF	PWMIF	--	TF4	TF3
R/W	R	R	--	R/W	R	--	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPIIF: SPI total interrupt instruction, Read only;
1= SPI interrupt, (Automatically cleared after clearing the specific interrupt flag);
0= No SPI interrupt.

Bit6 I2CIF: I^2C Total interrupt instruction, Read only;
1= I^2Cinterrupt, (Automatically cleared after clearing the specific interrupt flag);
0= No I^2Cinterrupt.

Bit5 --

Bit4 ADCIF: ADC interrupt flag;
1= ADC Conversion completed, need software clear;
0= ADC conversion is not complete.

Bit3 PWMIF: PWM Total interrupt instruction, Read only;
1= PWM interrupt, (Automatically cleared after clearing the specific interrupt flag);
0= No PWM interrupt.

Bit2 --

Bit1 TF4: Timer4 overflow interrupt flag;
1= Timer4 timer overflow, which is automatically cleared by hardware when entering the interrupt service routine, or can be cleared by software;
0= Timer4 has no overflow.

Bit0 TF3: Timer3 overflows interrupt flags;
1= Timer3 timer overflow, which is automatically cleared by hardware when entering the interrupt service routine, or can be cleared by software;
0= Timer3 has no overflow.

11.4 Timer3 Operation Mode

11.4.1 T3 - Mode0 (13-bit timing mode)

In this mode, Timer3 is 13-bit register. When all the '1' of the counter become '0', the interrupt flag bit TF3 is set to '1'. The 13-bit register consists of the lower 5 bits of TL3 and TH3. The higher 3 bits of TL3 should be ignored.

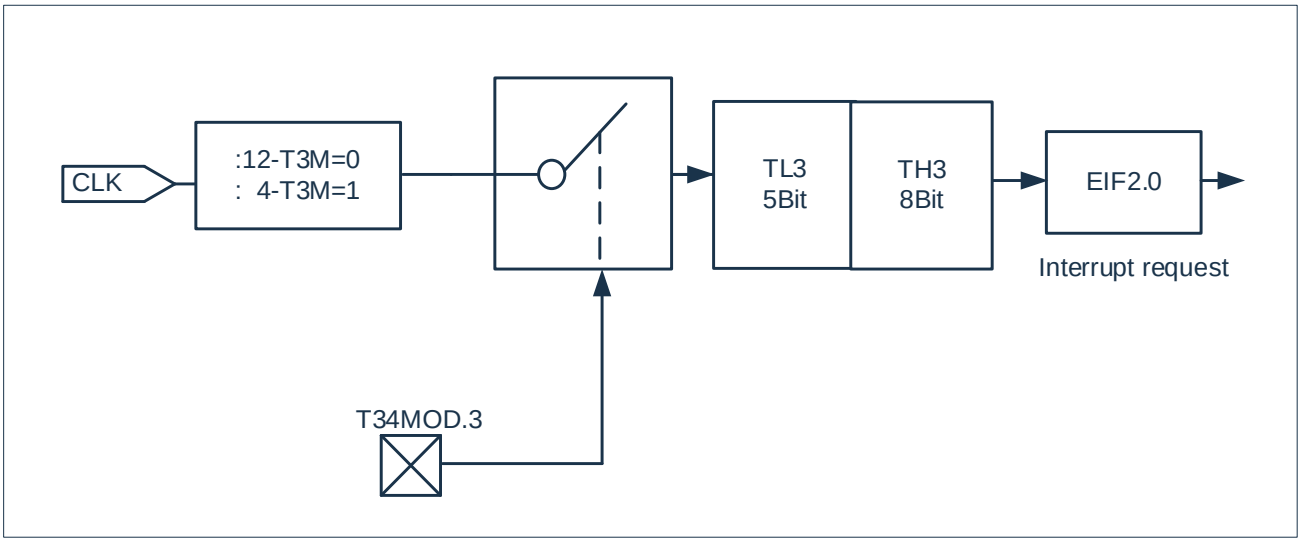


Figure 11-1: Timer3, Mode0: 13-bit Timer

11.4.2 T3 - Mode1 (16-bit timing mode)

Mode 1 is the same as mode 0, Just in mode 1,all 16 bits of the Timer3 register work. Mode 1 is shown below.

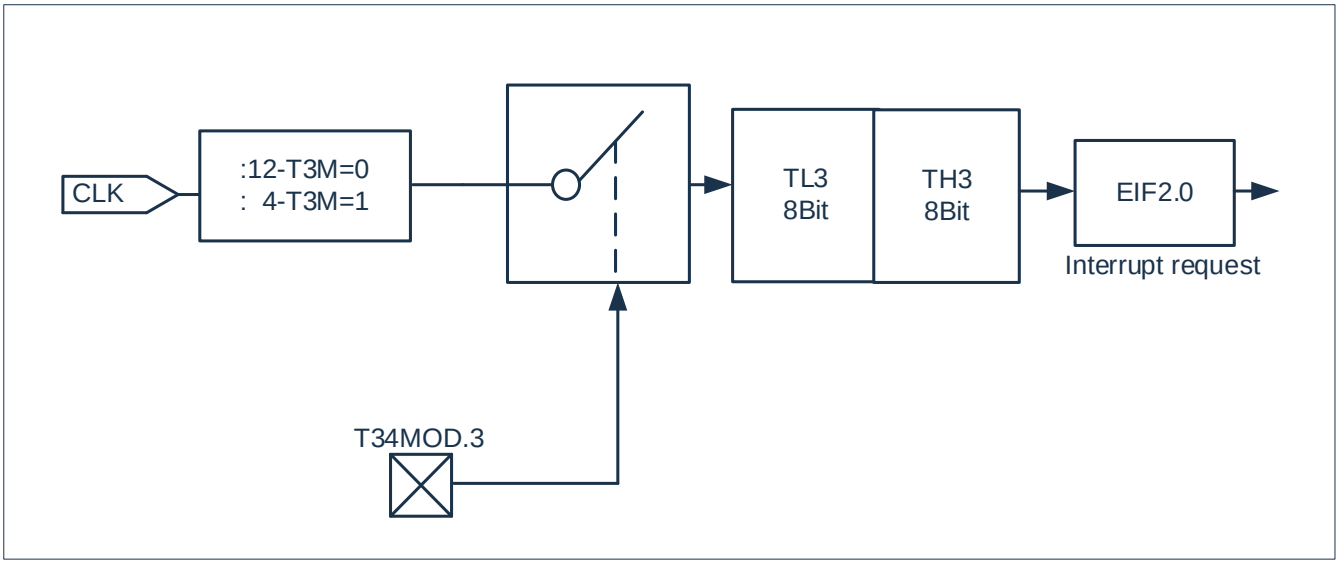


Figure 11-2: Timer3, Mode1: 16-bit Timer

11.4.3 T3 - Mode2 (8-bit automatic reload timing mode)

In mode 2, the Timer3 register is an 8-bit counter with automatic reload mode, as shown below. Overflow from TL3 register. Not only set TF3,but also reload TH3 to TL3,the value of TH3 remains unchanged during the reload process.

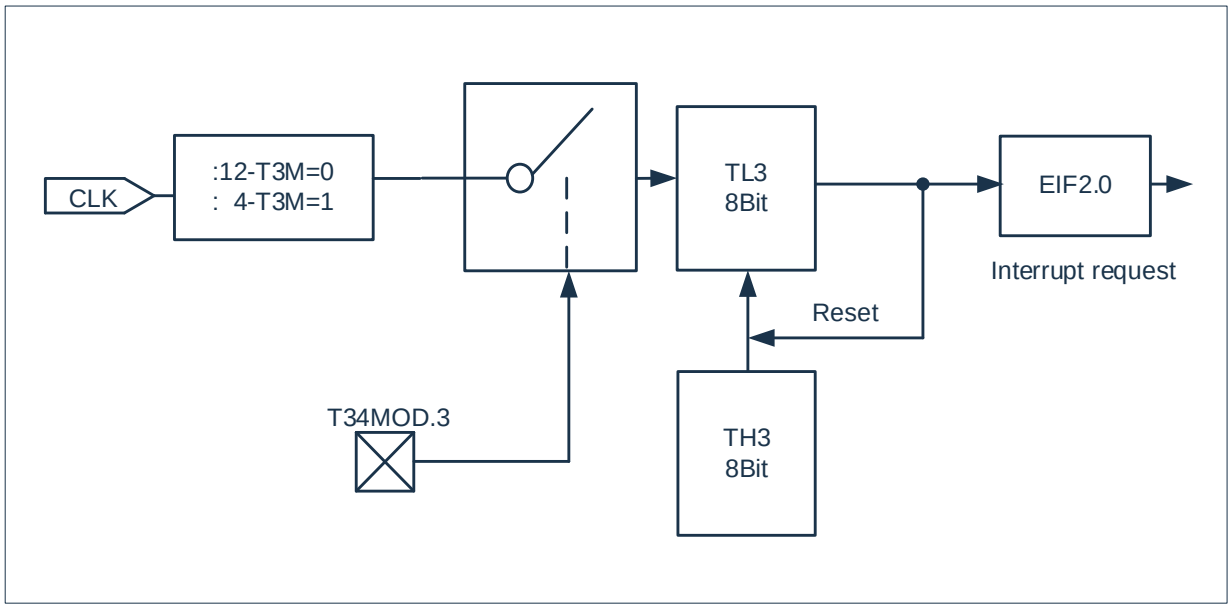


Figure 11-3: Timer3, Mode2: 8-bit Timer (automatic reload)

11.4.4 T3 - Mode3 (Two separate 8-bit timers)

In mode 3, times 3 sets TL3 and TH3 to two independent counters. The logic of mode3 of timer 3 is as follows.

TL3 works as an 8-bit timer, and use the control bit of timer 0: such as TR3 and TF3.

TH3 works as an 8-bit timer, use TR4 and TF4 flags and control the timer 4 interrupt.

When you need to use two 8-bit timers, you can use mode 3.When timer3 is in mode 3, timer4 can switch to itself, Mode 3 is turned off, or can still be used as a baud rate generator by the serial channel, or in any application that does not require Timer 4 interrupts.

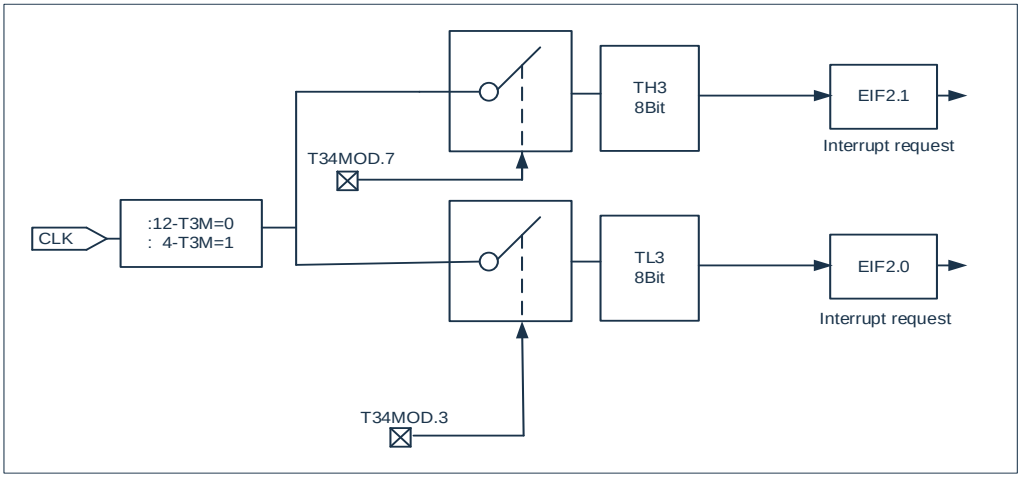


Figure 11-4: Timer3, Mode3: Two 8-bit Timers

11.5 Timer4 Working Mode

11.5.1 T4 - Mode0 (13-bit timing mode)

In this mode, timer 4 is a 13-bit register. When all the '1' of the counter become '0', the interrupt flag bit TF4 is set to '1'. The 13-bit register consists of the lower 5 bits of TL4 and TH4. The higher 3 bits of TL4 should be ignored.

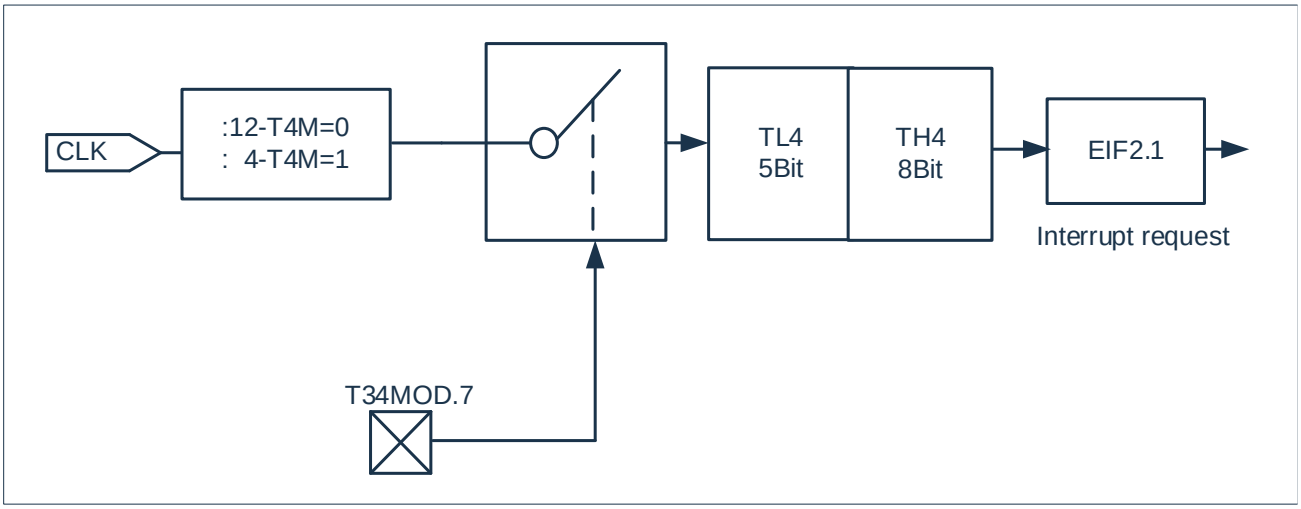


Figure 11-5: Timer4, Mode0: 13-bit timer

11.5.2 T4 - Mode1 (16-bit timing mode)

Mode 1 is the same as mode 0, Just in mode 1,all 16 bits of the Timer4 register work. Mode 1 is shown below.

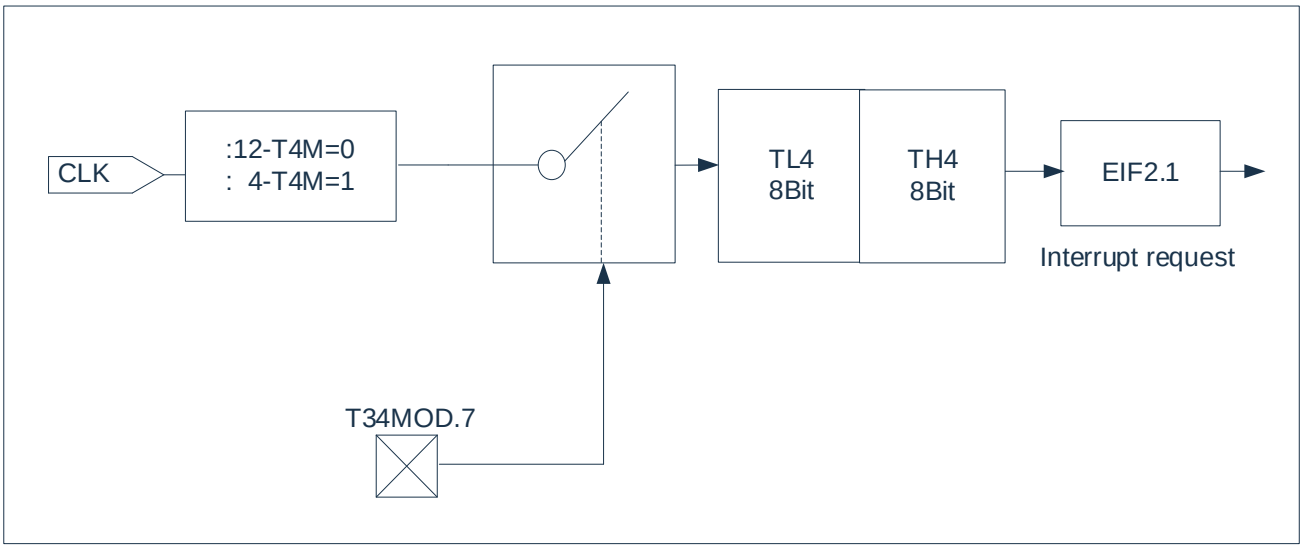


Figure 11-6: Timer4, Mode1: 16-bit timer/counter

11.5.3 T4 - Mode2 (8-bit automatic reload timing mode)

In mode 2, the Timer4 register is an 8-bit counter with automatic reload mode, as shown below. Overflow from TL4 register. Not only set TF4,but also reload TH4 to TL4,the value of TH4 remains unchanged during the reload process.

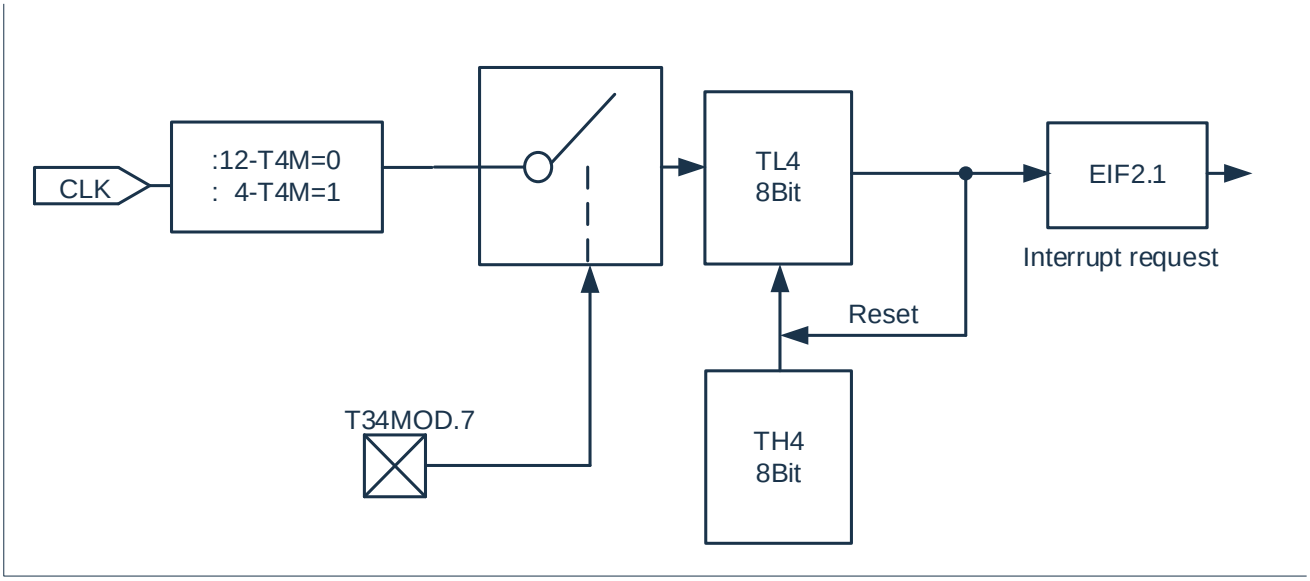


Figure 10-7: Timer4, Mode2: 8-bit timer (automatic reload)

11.5.4 T4 - Mode3 (stop counting)

Mode 3 stops counting, the effect is the same as setting TR4 = 0.

12. BUZZER

The buzzer consists of an 8-bit counter, a clock driver, and a control register. It produces a 50% duty cycle square wave, its frequency covers a wide range. The output frequency of BUZZER is controlled by the BUZCON register and the BUZDIV register.

When using the buzzer, you need to configure the relevant port (supports any GPIO) as a buzzer port first:

P24CFG = 0x18;// P2.4 configured as a buzzer port

BUZZER Control Register (BUZCON)

0xBF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BUZCON	BUZEN	--	--	--	--	--	BUZCKS1	BUZCKS0
R/W	R/W	R	R	R	R	R	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7	BUZEN:	BUZZER enable bit;
	1=	Enable;
	0=	Disable.
Bit6~ Bit2	--	
Bit1~ Bit0	BUZCKS<1:0>:	BUZZER frequency division ratio;
	00=	Fsys/8;
	01=	Fsys/16;
	10=	Fsys/32;
	11=	Fsys/64.

BUZZER Frequency Control Register (BUZDIV)

0xBE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BUZDIV	BUZDIV7	BUZDIV6	BUZDIV5	BUZDIV4	BUZDIV3	BUZDIV2	BUZDIV1	BUZDIV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0	BUZDIV<7:0>:	BUZZER frequency selection bit;
	0x00=	No square wave output;
	Others =	Fbuz =Fsys/(2*CLKDIV*BUZCKS).

Note: It is not recommended to modify BUZDIV when BUZEN=1.

Example 1: Fsys= 8MHz, BUZCKS<1:0>=01, BUZDIV=125
Fbuz=8MHz/(2*125)/16= 2KHz

Example 2: Fsys=16MHz, BUZCKS<1:0>=11, BUZDIV=125
Fbuz=16MHz/(2*125)/64= 1KHz

Example 3: Fsys=24MHz, BUZCKS<1:0>=11, BUZDIV=94
Fbuz=24MHz/(2*94)/64= 2KHz

Buzzer output frequency list

BUZCKS<1:0>	Fbuz@Fsys=8MHz	Fbuz@Fsys=16MHz	Fbuz@Fsys=24MHz
00	2KHz-500KHz	4KHz-1MHz	6KHz-1.5MHz
01	1KHz-250KHz	2KHz-500KHz	3KHz-750KHz
10	0.5KHz-125KHz	1KHz-250KHz	1.5KHz-375KHz
11	0.25KHz-62.5KHz	0.5KHz-125KHz	0.75KHz-187.5KHz

13. ANALOG To DIGITAL CONVERSION (ADC)

13.1 ADC Overview

The ADC can convert the analog input signal into a 12-bit binary value which indicates the signal. The analog input signal at the port is connected to the input of the analog to digital converter after passing through the multiliexer.ADC adopts a successive approximation method to produce a 12-bit binary result, and save the result in the ADC result register (ADRESL and ADRESH).

ADC reference voltage is always generatedinternally.ADC can generate an interrupt after the conversion is complete.

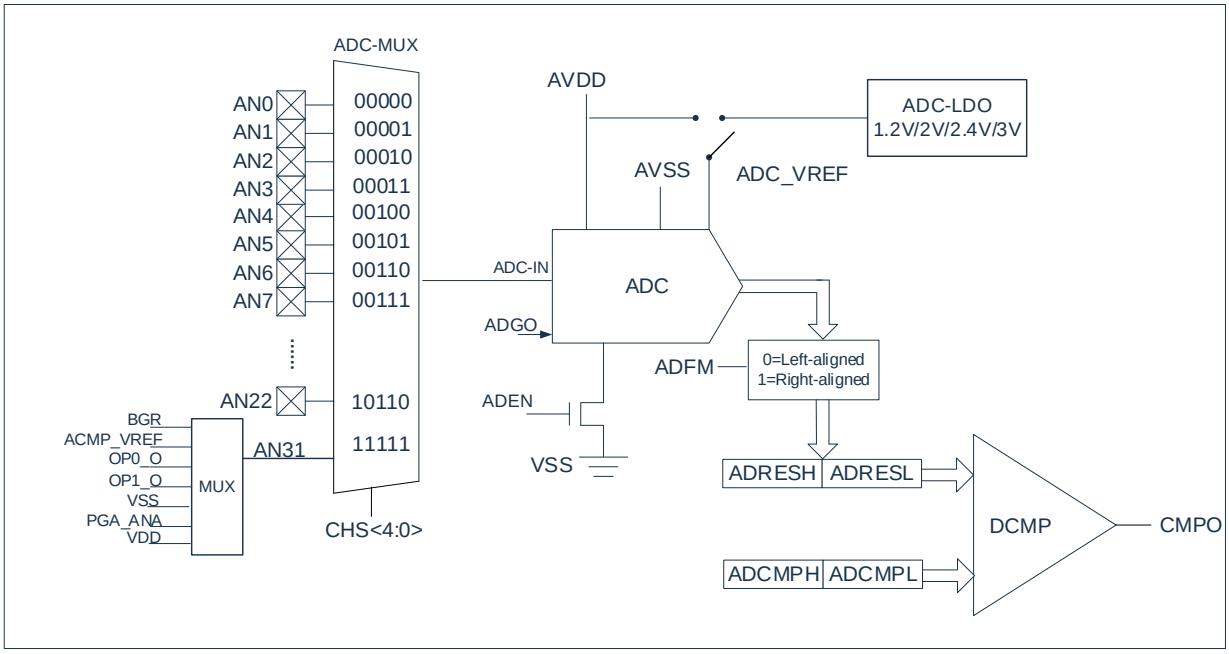


Figure 13-1: ADC block diagram

13.2 ADC Configuration

When configuring and using the ADC, the following factors must be considered:

- Port configuration;
- Channel selection;
- ADC conversion clock source;
- Interrupt control;
- Result storage format.

13.2.1 Port Configuration

The ADC can convert analog signals and convert digital signals. When converting analog signals, should be configured as an analog port by configuring the corresponding. See the corresponding port chapter for more information.

Note: Applying an analog voltage to a pin defined as a digital input may cause an over current in the input buffer.

13.2.2 Channel Selection

Which channel is connected to the analog-to-digital converter is determined by the ADCHS bit of the ADCON1 register.

If the channel is changed, a certain delay is required before the next conversion starts. The ADC delay time is shown in the table below.

Delay time	Operating voltage
500ns	2.5~4.5V
200ns	4.5~5.5V

For more information, please refer to “ADC Operating Principle”.

13.2.3 ADC Reference Voltage

The reference voltage of the ADC is provided by the VDD of the chip by default, or it can be provided by the internal ADC-LDO, which can choose 4 voltage outputs: 1.2V/2.0V/2.4V/3.0V.

13.2.4 Conversion Clock

The ADCKS bit of the ADCON1 register can be set by software to select the clock source for conversion.

The time to complete a one-bit conversion is defined as TADCK . A complete 12-bit conversion takes 18.5 TADCK cycles (the time to complete a conversion ADGO lasts as high).

The corresponding TADCK specification must be met in order to obtain the correct conversion results. The following table shows a reference example for selecting the ADC clock.

Fsys	FADCK (TA=25°C)		
	VREF=VREF1=AVDD (AVDD=VDD)	VREF=VREF2=1.2V	VREF=VREF3=2.0V VREF=VREF4=2.4V VREF=VREF5=3.0V
8MHz	Fsys/4	Fsys/256	Fsys/16
16MHz	Fsys/8	Disable	Fsys/32
24MHz	Fsys/16	Disable	Fsys/64
48MHz	Fsys/32	Disable	Fsys/128

Note: Any change in system clock frequency will change the frequency of the ADC clock, which will negatively affect the ADC conversion results.

13.2.5 ADC Interrupt

The ADC module allows an interrupt to be generated after the analog to digital conversion is completed. The ADC Interrupt Flag is the ADCIF bit in the EIF2 register. The ADC Interrupt Enable bit is the ADCIE bit in the EIE2 register. The ADCIF bit must be cleared in software. The ADCIF bit is set after each conversion and is independent of whether the ADC interrupt is enabled.

13.2.6 Result Formatting

The result of a 12-bit A/D conversion can be in two formats: left or right. The output format is controlled by the ADFM bit of the ADCON0 register.

- When ADFM=0, the AD conversion result is left aligned;
- When ADFM=1, the AD conversion result is right aligned.

13.3 ADC Hardware Triggered Start

In addition to the software-triggered AD conversion, the ADC module also provides a way to trigger the hardware, one for the external port edge trigger mode, one It is an edge or period trigger of PWM. Using hardware to trigger the ADC requires ADCEX to be set, even if the ADC function can be externally triggered. After a certain delay, the hardware trigger signal will automatically clear the ADGO bit after the conversion. When the hardware trigger function is enabled, the software trigger function will not be turned off. When the ADC is idle, writing 1 to the ADGO bit can also start AD conversion.

13.3.1 External Port Edge Trigger ADC

The ADCETn pin edge automatically triggers an AD conversion. At this time ADTGS[1:0] needs to be 11 (select external port edge trigger), and ADEGS[1:0] can select which edge trigger.

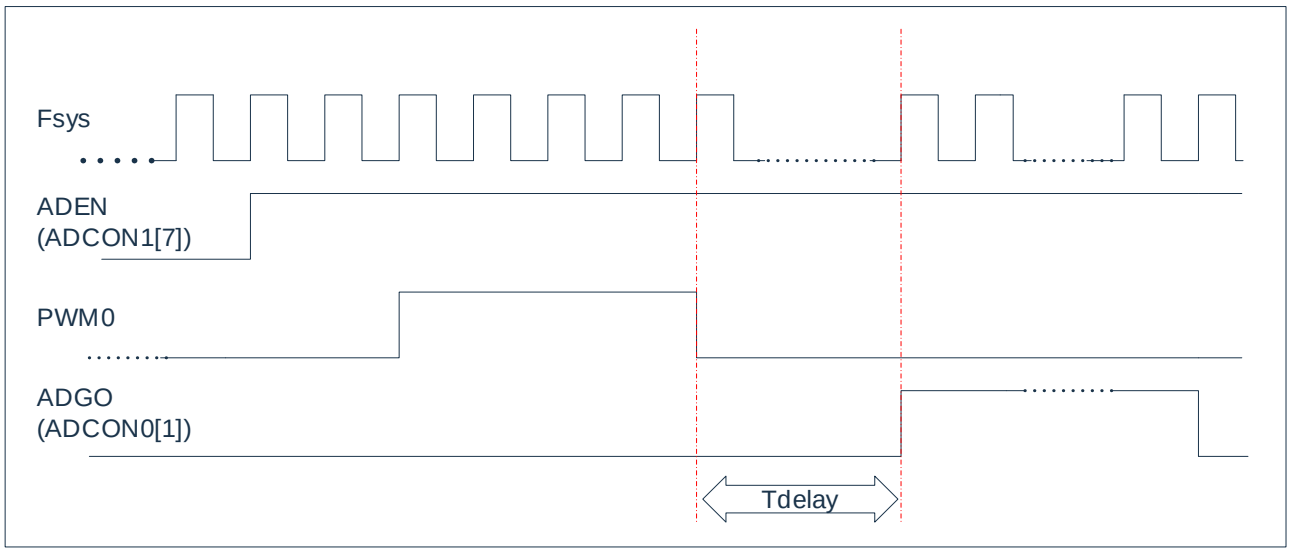
13.3.2 PWM Triggered ADC

The PWM selects whether the ADC conversion is triggered by an edge or a period zero/midpoint. ADTGS[1:0] selects the PWM channel (PG0, PG2, PG4), and ADEGS[1:0] can select the edge type or period type trigger mode.

13.3.3 Hardware Trigger Delay Before Starting

After the hardware trigger signal is generated, the AD conversion is not started immediately. It takes a certain delay before the ADGO value is set to 1. Delay by ADDLY[9:0] decided.

Delay time of hardware trigger signal: Tdelay = (ADDLY+3)*Tsys



13.4 ADC Operating Principle

13.4.1 Start Conversion

To enable the ADC module, the ADEN bit of the ADCON1 register must be set and then the analog-to-digital conversion is initiated by setting the ADGO bit of the ADCON0 register (ADGO cannot be set to 1 when ADEN is '0').

13.4.2 Complete Conversion

When the conversion is complete, the ADC module will:

- Clear ADGO bit;
- Set ADCIF bit 1;
- Update the ADRESH:ADRESL register with the new result of the conversion.

13.4.3 Terminate Conversion

After the ADC is started, you must wait for the ADC conversion to be completed before terminating the ADC conversion, and it is prohibited to terminate the ADC conversion during the ADC conversion.

Note: A device reset will force all registers to the reset state. Therefore, reset will turn off the ADC module and terminate any pending conversions.

13.4.4 A/D Conversion Steps

The ADC use age guide is given as follows step by step:

1. Pin configuration:
   - Use a pin as a driver is forbidden (PxTRIS register);
   - Configure pins as analog input pin.
2. Configure ADC block:
   - Choose ADC conversion clock;
   - Choose ADC input channel;
   - Choose the format of results;
   - Initiate ADC block
3. Configure ADC interrupt (optional):
   - Reset ADC interrupt flag bit;
   - Enable ADC interrupt;
   - Enable peripheral interrupt;
   - Enable global interrupt.
4. Waiting for the required sampling time.
5. Set ADGO to 1 to initiate conversion.
6. Waiting for the end of conversion by one of the following ways:
   - Check ADGO bit;
   - Waiting for the ADC interrupt (enable interrupt).
7. Read ADC Results.
8. Reset the ADC flag bit of interrupt (This step is required to be done if interrupt is enabled).

Note: If a customer is trying to renew the device's sequence code execution after it's awakened from sleep mode, then global interrupt must be forbidden.

13.4.5 Conversion During Sleep Mode

When the system is about to sleep, it's must wait for the conversion is completed, and then getting into sleep mode. It is forbidden to put the chip into sleep during ADC conversion.

13.5 ADC Related Registers

The following ten registers are related to AD conversion:

- AD control registers: ADCON0, ADCON1, ADCON2, ADCLDO;
- Comparator control register: ADCMPC;
- Delay data register: ADDLYL;
- AD results data registers:ADRESH/L;
- Comparator data register: ADCMPH/L.

AD Control Register (ADCON0)

0xDF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON0	ADCHS4	ADFM	--	AN31SEL2	AN31SEL1	AN31SEL0	ADGO	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7	ADCHS4	Bit 4 of the ADC analog channel selection bit;
	1=	Selection of channel assignments refer to the description in register ADCON1 below;
	0=	--
Bit6	ADFM:	ADC conversion result format selection bit;
	1=	Right alignment;
	0=	Left alignment.
Bit5	--	Reserved
Bit4~Bit2	AN31SEL<2:0>:	ADC channel 31 input source selection bit;
	000=	BGR (1.2V);
	001=	ACMP_VREF (comparator negative reference voltage, see ACMP chapter for details);
	010=	OP0_O;
	011=	OP1_O;
	100=	PGA_ANA (PGA internal output signal, see chapter PGA module for details);
	101=	VSS (ADC reference ground);
	110=	Reserved, disable use;
	111=	VDD (ADC default reference voltage).
Bit1	ADGO:	ADC conversion start bit (ADEN must be 1 when setting 1 to this bit, otherwise the operation is invalid);
	1=	Write: start of ADC conversion, (hardware triggering of ADC will also set this bit to 1). Read: ADC is converting.
	0=	Write to: Invalid. Read: ADC idle/conversion complete. During the conversion of the ADC (ADGO=1), any software and hardware trigger signals will be ignored.
Bit0	--	

AD Control Register (ADCON1)

0xDE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON1	ADEN	ADCKS2	ADCKS1	ADCKS0	ADCHS3	ADCHS2	ADCHS1	ADCHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	1	0	0	0	0	0	0

Bit7 ADEN: ADC enable bit;
1= Enable ADC;
0= Disable ADC, no operating current is consumed.

Bit6~Bit4 ADCKS<2:0>: ADC conversion clock select bit.

000=	Fsys/2	100=	Fsys/32
001=	Fsys/4	101=	Fsys/64
010=	Fsys/8	110=	Fsys/128
011=	Fsys/16	111=	Fsys/256

Bit3~Bit0 ADCHS<3:0>: The analog channel select bits are 4 bits lower and form a 5-bit channel select bit with ADCHS<4>, ADCHS<4:0>;

00000=	AN0	10000=	AN16
00001=	AN1	10001=	AN17
00010=	AN2	10010=	AN18
00011=	AN3	10011=	AN19
00100=	AN4	10100=	AN20
00101=	AN5	10101=	AN21
00110=	AN6	10110=	AN22
00111=	AN7	Other=	--
01000=	AN8	11111=	See the description of ADCON0.AN31SEL
01001=	AN9		
01010=	AN10		
01011=	AN11		
01100=	AN12		
01101=	AN13		
01110=	AN14		

AD Control Register (ADCON2)

0xE9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON2	ADCEX	--	ADTGS1	ADTGS0	ADEGS1	ADEGS0	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7	ADCEX:	ADC hardware trigger enable bit.
	1=	Enable;
	0=	Disable.
Bit6	Reserved:	It must be 0.
Bit5~Bit4	ADTGS<1:0>:	ADC hardware trigger source select bit;
	00=	PG0(PWM0);
	01=	PG2 (PWM2);
	10=	PG4 (PWM4);
	11=	Port pin (ADET).
Bit3~ Bit2	ADEGS<1:0>:	A DC hardware trigger edge select bit;
	00=	Falling edge;
	01=	Rising edge;
	10=	The period point of the PWM cycle;
	11=	The zero point of the PWM period.
Bit1~Bit0	--	

AD Comparator Control Register (ADCMPC)

0xD1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCMPC	ADFBEN	ADCMPPS	--	ADCMPO	--	--	ADDLY9	ADDLY8
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7	ADFBEN:	The result of ADC comparator controls PWM brake enable bit;
	1=	Enable;
	0=	Disable.
Bit6	ADCMPPS:	The output polarity of ADC comparator select bit;
	1=	If ADRES<ADCMP, then ADCMPO=1;
	0=	If ADRES>=ADCMP, then ADCMPO=1.
Bit5	--	
Bit4	ADCMPO:	ADC comparator output bit (read only). This bit outputs ADC comparator's result, it'll be updated every time ADC 's conversion is completed.
Bit3~Bit2	--	
Bit1~ Bit0	ADDLY[9:8]:	ADC hardware trigger delay data[9:8]bits.

AD Hardware Trigger Delay Data Register (ADDLYL)

0xD3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDLYL	ADDLY7	ADDLY6	ADDLY5	ADDLY4	ADDLY3	ADDLY2	ADDLY1	ADDLY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 ADDLY<7:0>: ADC hardware trigger delay data lower 8 bits.

AD Data Register Higher Bits: ADRESH, ADFM=0 (left-aligned)

0xDD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADRESH	ADRES11	ADRES10	ADRES9	ADRES8	ADRES7	ADRES6	ADRES5	ADRES4
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 ADRES<11:4>: ADC results register bits.
Number 11 to 4 bit of 12 bits conversion results.

AD Data Register Lower Bits: ADRESL, ADFM=0 (left-aligned)

0xDC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADRESL	ADRES3	ADRES2	ADRES1	ADRES0	--	--	--	--
R/W	R	R	R	R	--	--	--	--
Reset value	X	X	X	X	--	--	--	--

Bit7~Bit4 ADRES<3:0>: ADC results register bits.
Number 3 to 0 bit of 12 bits conversion results.
Bit3~Bit0 Not used.

AD Data Register Higher Bits: ADRESH, ADFM=1 (Right-Aligned)

0xDD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADRESH	--	--	--	--	ADRES11	ADRES10	ADRES9	ADRES8
R/W	--	--	--	--	R	R	R	R
Reset value	--	--	--	--	X	X	X	X

Bit7~Bit4 Not used.
Bit3~Bit0 ADRES<11:8>: ADC results register bits.
Number 11 to 8 bit of 12 bits conversion results.

AD Data Register Lower Bits: ADRESL, ADFM = 1 (Right-Aligned)

0xDC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADRESL	ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 ADRES<7:0>: ADC results register bits.
Number 7 to 0 bit of 12 bits conversion results.

AD Comparator Data Register (ADCMPH)

0xD5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCMPH	D11	D10	D9	D8	D7	D6	D5	D4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit7~Bit0 ADCMP<11:4>: Higher 8 bits of ADC comparator's data.

AD Comparator Data Register (ADCMPL)

0xD4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCMPL	--	--	--	--	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit7~Bit4 Not used.

Bit 3~Bit0 ADCMP[3:0]: Lower 4 bits of ADC comparator's data.

ADCReference Voltage Control Register (ADCLDO)

F692H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCLDO	LDOEN	VSEL1	VSEL0	--	--	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 LDOEN ADC_LDO enable.

1= LDO enable, the reference voltage can be selected only for the voltage corresponding to VSEL[1:0].

0= LDO is disabled and the reference voltage is the chip supply voltage.

Bit 6~Bit5 VSEL[1:0]: ADC reference voltage selection bit.

00= 1.2V;.

01= 2.0V;.

10= 2.4V;.

11= 3.0V .

Bit4 -- Reserved, must be 0.

Bit 3~Bit0 --

13.6 ADC Results Comparison

ADC block provides a set of digital comparators for comparison between the results of ADC and the numbers pre-loaded in {ADCMPH,ADCMPL}.The conversion results of ADC will be compared with preset value ADCMP every time, the result of comparison will be stored in ADCMPO flag bit, this flag bit will updated automatically after the conversion. ADCCMPPS bit could change the polarity of the output results.

ADC comparison result could trigger PWM fault brake; it requires to set ADFBEN to 1 if enabling this function.

When PWM function is enabled, when ADFBEN=1,the conversion results of ADC will be compared with preset value {ADCMPH,ADCMPL},if the comparison result is 1,PWM generates fault brake action, resets all the PWM channels and terminates all the outputs of PWM channels.

14. ENHANCED PWM MODULE

14.1 Overview

The PWM0 supports six PWM generators which can be configured as six independent PWM outputs, (PG0-PG5), or as three complementary PWM pairs (PG0-PG1,PG2-PG3,PG4-PG5)with three programmable dead-time generators.

Every complementary PWM pairs share one 8-bit prescaler, There are six clock dividers providing five divided frequencies (1, 1/2, 1/4, 1/8, 1/16) for each channel. Each PWM output has independent 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The six PWM generators provide twenty-four independent PWM interrupt flags, corresponding period or duty cycle of PWM channel is matched with counter, interrupt flag will be generated, each PWM posses its own independent enable bit.

Each PWM generator can be configured as One-shot mode to produce only one PWM cycle signal or loop mode to output PWM waveform continuously.

14.2 Features

Enhanced PWM supports the following features:

- Six independent 16-bit PWM control mode.
  - Six independent outputs - PG0,PG1,PG2,PG3,PG4,PG5;
  - Three complementary PWM pairs: (PG0-PG1), (PG2-PG3), (PG4-PG5),capable of programmable dead-time insertion;
  - Three synchronous PWM pairs: (PG0-PG1), (PG2-PG3), (PG4-PG5),with each pin in a pair in-phase.
- Support group control, the outputs of PG0 and PG2 and PG4 are synchronized, the outputs of PG1 and PG3 and PG5are synchronized.
- One-shot(only support edge-aligned type) or Auto-reload mode PWM.
- Support edge-aligned mode and center-aligned mode.
- Support symmetrical and asymmetrical counting in center-aligned mode.
- Support programmable dead-time generator between complementary paired PWMs.
- Each PWM generator has independent polarity setting control.
- Hardware fault brake protections (external FB1 trigger, support software trigger).
- ADC comparing event triggers hardware fault brake protection.
- PWM edge or period triggers to start AD conversion.

14.3 Port Configuration

Before using the enhanced PWM module, you need to configure the corresponding port as PWM channel (any GPIO can be configured as PWM channel), PWM channels are marked with PG0-PG5 on the multiplexed function assignment diagram, corresponding to PWM channels 0-5 respectively.

The assignment of PWM channels is controlled by the corresponding port configuration registers, for example.

```
P13CFG=0x12;// Configure P13 as PG0 channel
P14CFG=0x13;// Configure P14 as PG1 channel
P15CFG=0x14;// Configure P15 as PG2 channel
P16CFG=0x15;// Configure P16 as PG3 channel
P17CFG=0x16;// Configure P17 as PG4 channel
P22CFG=0x17;// Configure P22 as PG5 channel
```

14.4 Function Description

It supports two kinds of operating mode: edge-aligned, center-aligned.

14.4.1 Edge-Aligned

In Edge-aligned PWM Output type, the 16-bit PWM counter CNTn will start counting-down from the start of every period, compare with the latched value of CMPn, PGn will output high level voltage when CNTn=CMPn, CMPnDIF is set to 1.CNTn continues counting-down to zero, PGn will output low voltage at this moment, also CMPn and PERIODn will be updated in the condition of PWMnCNTM=1,PIFand set PIF period interrupt flag.

Edge-aligned corresponding parameters:

$$\text{High level time} = (\text{CMPn}+1)\times T_{pwm}\ (\text{CMPn}\geq 1)$$

$$\text{Period} = (\text{PERIODn}+1)\times T_{pwm}$$

$$\text{Duty cycle} = \frac{\text{CMPn}+1}{\text{PERIODn}+1}\ (\text{CMPn}\geq 1)$$

The duty cycle is 0% when CMPn=0.

The edge alignment timing is shown in the following figure:

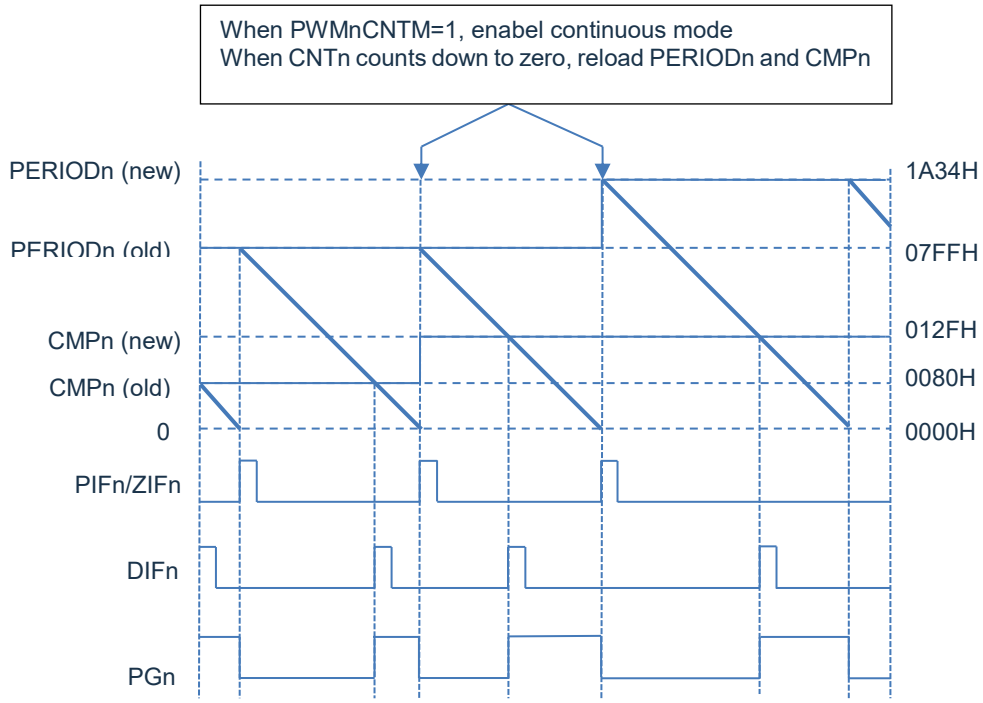


Figure 14-1: Edge-aligned timing diagram

14.4.2 Center-Aligned

In the center-aligned symmetric counting mode, the 16-bit PWM counter CNTn starts counting up from 0. When CNTn=CMPn, PGn outputs high, after which CNTn continues to count up until it is equal to PERIODn, and then CNTn starts counting down, and in the process of counting down when CNTn=CMPn, PGn outputs low, after which it continues to count down to 0.

The parameters related to the center-aligned symmetric counting method are as follows:

$$\text{high level time} = (PERIODn \times 2 - CMPn \times 2 - 1) \times Tpwm\ ;\ (CMPn \geq 1)$$

$$period = (PERIODn) \times 2 \times Tpwm\ ;$$

$$duty\ cycle = \frac{PERIODn \times 2 - CMPn \times 2 - 1}{PERIODn \times 2}\ ;\ (CMPn \geq 1)$$

100% duty cycle when CMPn=0;

The center-aligned timing (symmetric counting) is shown in the following figure:

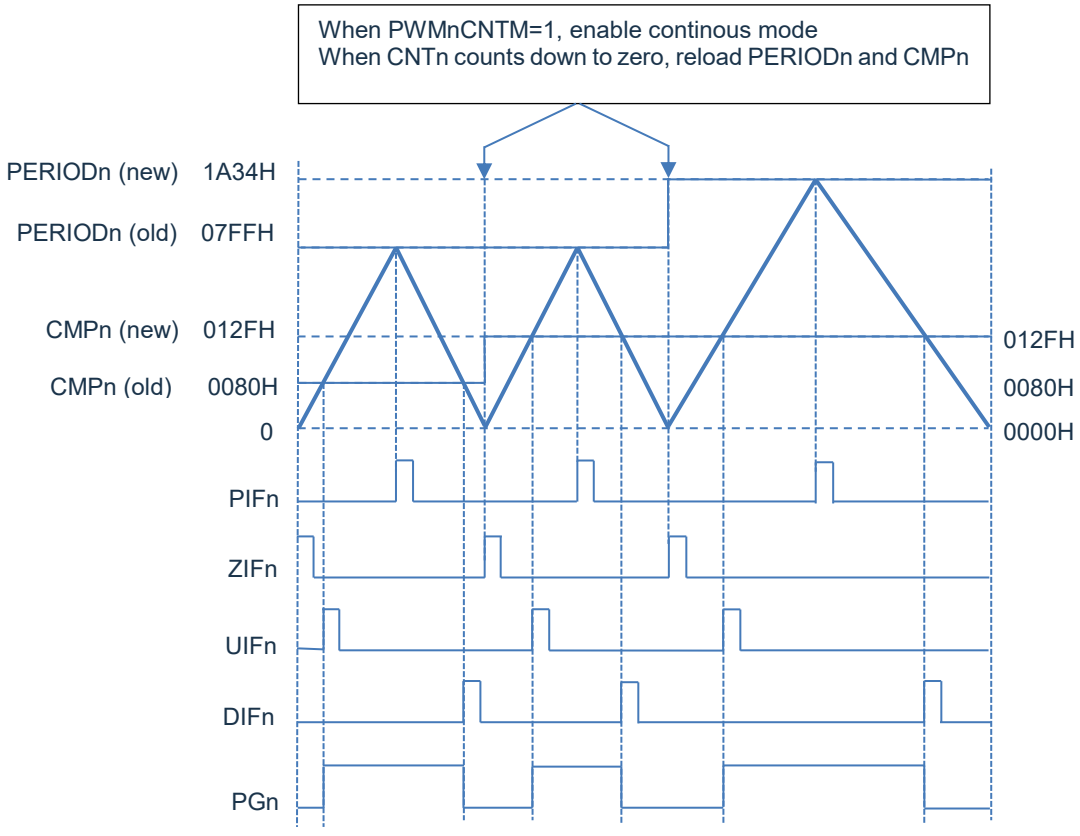


Figure 14-2: Center-aligned timing diagram (symmetrical counting)

Figure 14-3 shows the waveform of center-aligned counter:

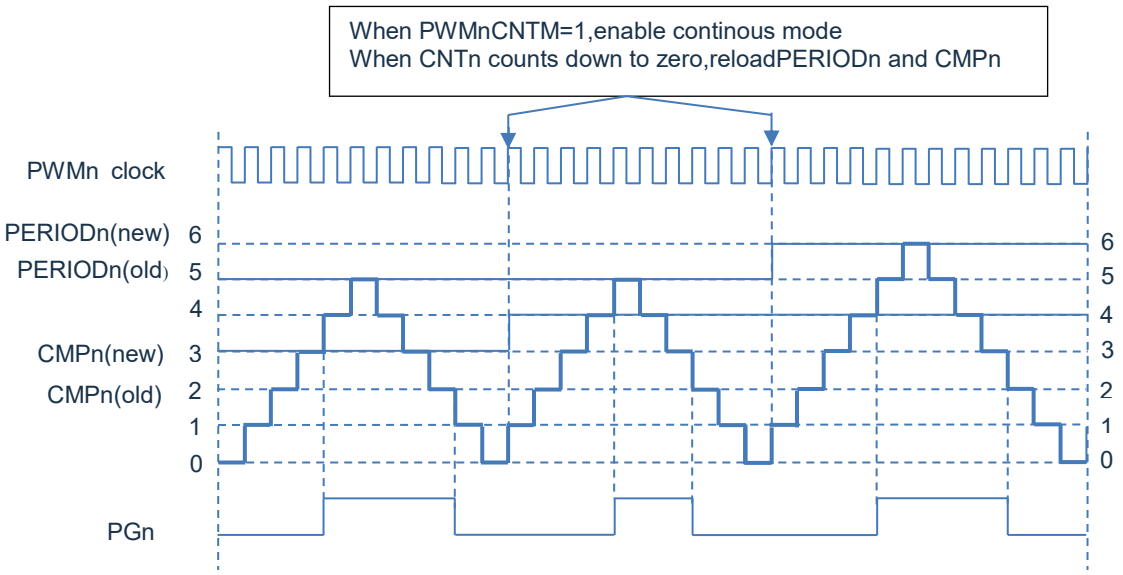


Figure 14-3: Center-aligned counter waveform (symmetrical counting)

In the center-aligned asymmetric counting mode, the 16-bit PWM counter CNTn starts counting upward from 0. When CNTn=CMPn, PGn outputs high, after which CNTn continues to count upward until it is equal to PERIODn, and then CNTn starts counting downward. To turn on the asymmetric counting mode, set ASYMEN to 1. The asymmetric counting mode can achieve accurate center-aligned waveforms.

The parameters related to the center-aligned asymmetric counting method are as follows:

$$High\ level\ time = (PERIODn \times 2 - CMPDn - CMPn - 1) \times Tpwm$$

$$Period = (PERIODn) \times 2 \times Tpwm$$

$$Duty\ cycle = \frac{PERIODn \times 2 - CMPDn - CMPn - 1}{PERIODn \times 2}$$

C100% duty cycle when CMPn=0 and CMPDn=0;

The center-aligned timing (asymmetric counting) is shown in the following figure:

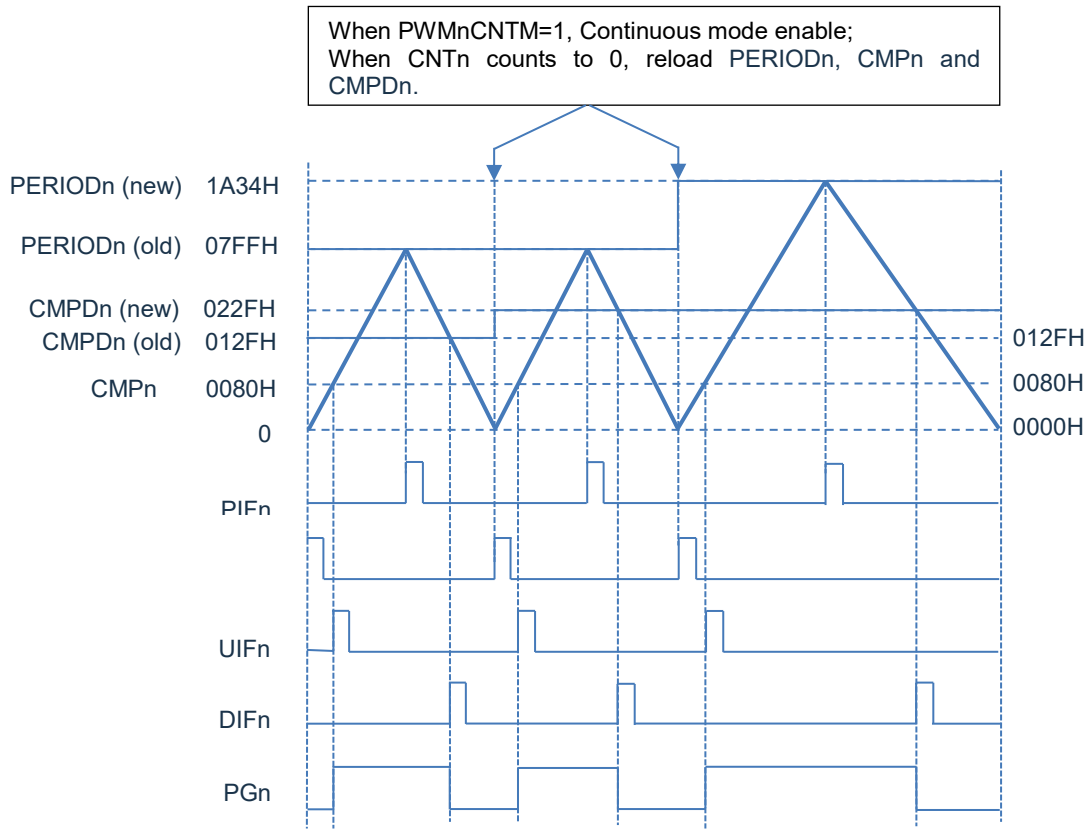


Figure 14-4: Centre-aligned timing diagram(Asymmetric counting)

Centre alignment timeline diagram (Asymmetric count) is shown in the figure below:

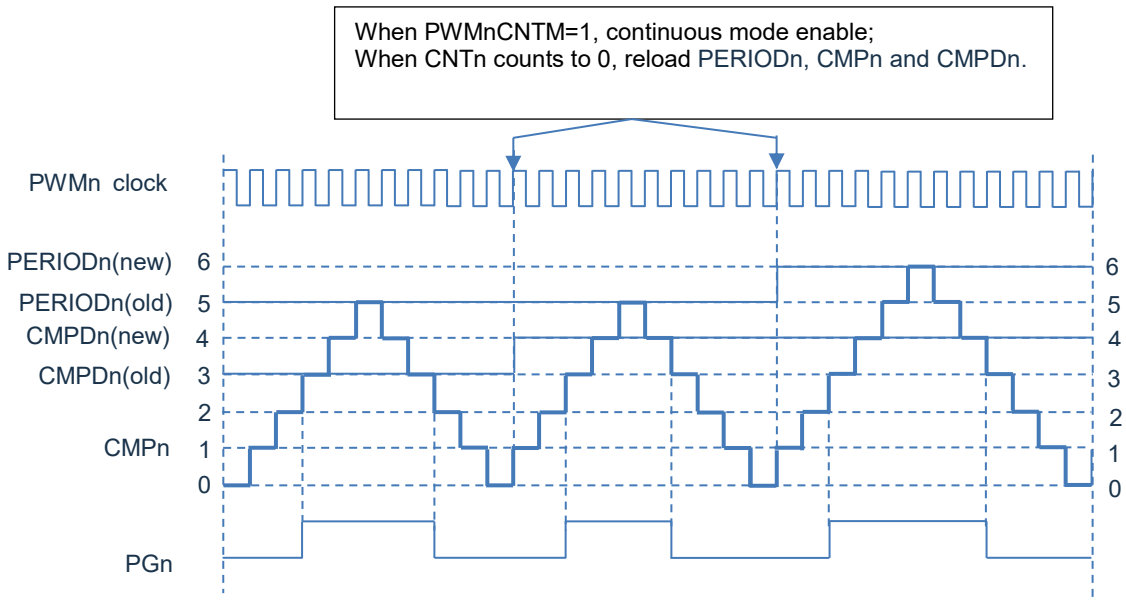


Figure 14-5: Centre alignment timing diagram (Asymmetric count)

14.4.3 Complementary Mode and Dead Zone Delay

6 channel PWM can be set to 3 sets of complementary pairs. In the complementary mode, the period and duty cycle of PWM1, PWM3 and PWM5 are determined by the relevant registers of PWM0, PWM2 and PWM4 respectively. Meanwhile, the dead zone delay register can also affect the duty cycle of PWM complementary pair. At this point, in addition to the corresponding output enabling bit (PWMnOE), PWM1/PWM3/PWM5 output waveform is no longer controlled by its own registers.

In complementary mode, each of PWM complementary pairs support insert dead zone delay. Insert dead zone time as follows:

PWM0/1 dead zone time: (PWM01DT+1) *T_{PWM0}

PWM2/3 dead zone time: (PWM23DT+1) *T_{PWM2}

PWM4/5 dead zone time: (PWM45DT+1) *T_{PWM4}

T_{PWM0}/T_{PWM2}/T_{PWM4} are clock source cycles of PWM0/PWM2/PWM4, respectively.

Both center alignment and edge alignment support complementary patterns.

14.4.4 Brake Function

There are several sources that trigger PWM brakes:

1. External trigger port FB;
2. ADC result compare output;

After the brake is triggered, the brake flag is set to 1, the counter enable bit of all channels is cleared, and the PWM outputs the preset brake data.

To resume normal output, you need to clear the brake flag and re-enable the PWM channel counter.

14.5 PWM Related Registers

PWM Control Register (PWMCON)

F120H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON	--	--	PWMMODE1	PWMMODE0	GROUPEN	ASYMEN	CNTTYPE	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit6 --

Bit5~Bit4 PWMMODE: Control bit of PWM's mode;
00= Independent mode;
01= Complementary mode;
10= Synchronize mode;
11= Reserved.

Bit3 GROUPEN: PWM group function enable bit;
1= PG0controlPG2,PG4;PG1 controlPG3,PG5;
0= All PWM Channel signal are independent of each other.

Bit2 ASYMEN: Asymmetric count enable bit in PWM center alignment;
1= Asymmetric counting is enabled;
0= Symmetric counting is enabled.

Bit1 CNTTYPE: PWM count alignment select bit;
1= Center alignment;
0= Edge alignment.

Bit0 --

PWM Output Enable Control Register (PWMOE)

F121H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWNOE	--	--	PWM5OE	PWM4OE	PWM3OE	PWM2OE	PWM1OE	PWM0OE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --

Bit5 PWM5OE: Output enable bit of PWM channel 5;
1= Enable;
0= Disable.

Bit4 PWM4OE: Output enable bit of PWM channel 4;
1= Enable;
0= Disable.

Bit3 PWM3OE: Output enable bit of PWM channel 3;
1= Enable;
0= Disable.

Bit2 PWM2OE: Output enable bit of PWM channel 2;
1= Enable;
0= Disable.

Bit1 PWM1OE: Output enable bit of PWM channel 1;
1= Enable;
0= Disable.

Bit0 PWM0OE: Output enable bit of PWM channel 0;
1= Enable;
0= Disable.

PWM0/1 Clock Prescaler Control Register (PWM01PSC)

F123H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM01PSC	PWM01PSC7	PWM01PSC6	PWM01PSC5	PWM01PSC4	PWM01PSC3	PWM01PSC2	PWM01PSC1	PWM01PSC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 PWM01PSC<7:0>: Prescaler control bit of PWM channel 0/1;
00= Prescaler clock stop, PWM0/1counter stop;
others = System clock (PWM01PSC+1) frequency divide.

PWM2/3 Clock Prescaler Control Register (PWM23PSC)

F124H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM23PSC	PWM23PSC7	PWM23PSC6	PWM23PSC5	PWM23PSC4	PWM23PSC3	PWM23PSC2	PWM23PSC1	PWM23PSC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 PWM23PSC<7:0>: Prescaler control bit of PWM channel 2/3;
00= Prescaler clock stop, PWM2/3 counter stop;
others = System clock (PWM23PSC+1)frequency divide.

PWM4/5 Clock Prescaler Control Register (PWM45PSC)

F125H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM45PSC	PWM45PSC7	PWM45PSC6	PWM45PSC5	PWM45PSC4	PWM45PSC3	PWM45PSC2	PWM45PSC1	PWM45PSC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 PWM45PSC<7:0>: Prescaler control bit of PWM channel 4/5;
00= Prescaler clock stop, PWM4/5counter stop;
others = System clock (PWM45PSC+1) frequency divide.

PWM Clock Frequency Division Control Register (PWMnDIV) (n=0-5)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMnDIV	--	--	--	--	--	PWMnDIV2	PWMnDIV1	PWMnDIV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register PWMnDIV(n=0-5) address: F12AH, F12BH, F12CH, F12DH, F12EH, F12FH.

Bit7~Bit3 --
Bit2~Bit0 PWMnDIV<2:0>: Clock frequency divide control bit of PWM channel n;
000= Fpwmn-PSC/2;
001= Fpwmn-PSC/4;
010= Fpwmn-PSC/8;
011= Fpwmn-PSC/16;
100= Fpwmn-PSC;
others = Fsys (system clock);
(PSC is the prescalered clock)

PWM Data Load Enable Control Register (PWMLOADEN)

F129H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMLOADEN	--	--	PWM5LE	PWM4LE	PWM3LE	PWM2LE	PWM1LE	PWM0LE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit6 --

Bit5~ Bit0 PWMnLE: Data load enable control register of PWM channel n(n=0-5)
(Hardware clear 0 when loading is finished);
1= Enable load period and duty period data (PERIODn, CMPn, CMPDn).
0= Writing 0 is invalid.

PWM Output Polarity Control Register (PWMPINV)

F122H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMPINV	--	--	PWM5PINV	PWM4PINV	PWM3PINV	PWM2PINV	PWM1PINV	PWM0PINV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit6 --

Bit5~ Bit0 PWMnPINV: Output polarity control bit of PWM channel n(n=0-5);
1= Inverse output;
0= Normal output.

PWM Counter Mode Control Register (PWMCNTM)

F127H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCNTM	--	--	PWM5CNTM	PWM4CNTM	PWM3CNTM	PWM2CNTM	PWM1CNTM	PWM0CNTM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit6 --

Bit5~ Bit0 PWMnCNTM: PWM channel n counter mode control bits (n=0-5);
1= Automatic loading mode;
0= One-shot mode.

PWM Counter Enable Control Register (PWMCNTE)

F126H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCNTE	--	--	PWM5CNTE	PWM4CNTE	PWM3CNTE	PWM2CNTE	PWM1CNTE	PWM0CNTE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit6 --

Bit5~ Bit0 PWMnCNTE: PWM channel n counter enable control bit (n=0-5);
1= PWMn counter on (PWMn starts output);
0= PWMn counter stops (software writes 0 to stop the counter and clear the counter value).

PWM Counter Mode Control Register (PWMCNTCLR)

F128H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCNTCLR	--	--	PWM5CNTCLR	PWM4CNTCLR	PWM3CNTCLR	PWM2CNTCLR	PWM1CNTCLR	PWM0CNTCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit6 --

Bit5~ Bit0 PWMnCNTCLR: PWM channel n is counter clear 0 control bit (n=0-5)
(Hardware clear 0 automatically);
1= PWMn counter clear 0;
0= Writing 0 is invalid.

PWM Period Data Low 8-bit Register (PWMPnL)(n=0-5)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMPnL	PWMPnL7	PWMPnL6	PWMPnL5	PWMPnL4	PWMPnL3	PWMPnL2	PWMPnL1	PWMPnL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register PWMPnL (n=0-5) address:F130H, F132H, F134H, F136H, F138H, F13AH.

Bit7~ Bit0 PWMPnL<7:0>: PWM channel n is period data low 8-bit register.

PWM Period Data High 8-bit Register (PWMPnH)(n=0-5)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMPnH	PWMPnH7	PWMPnH6	PWMPnH5	PWMPnH	PWMPnH3	PWMPnH2	PWMPnH1	PWMPnH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register PWMPnH (n=0-5) address: F131H, F133H, F135H, F137H, F139H, F13BH.

Bit7~ Bit0 PWMPnH<7:0>: PWM channel n is period data high 8-bit register.

PWM Compare Data Low 8-bit Register (PWMDnL)(n=0-5)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMDnL	PWMDnL7	PWMDnL6	PWMDnL5	PWMDnL4	PWMDnL3	PWMDnL2	PWMDnL1	PWMDnL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register PWMDnL (n=0-5) address: F140H, F142H, F144H, F146H, F148H, F14AH.

Bit7~ Bit0 PWMDnL<7:0>: PWM channel n is compare date (duty cycle data) low 8-bit register.

PWM Compare Data High 8-bit Register (PWMDnH)(n=0-5)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMDnH	PWMDnH7	PWMDnH6	PWMDnH5	PWMDnH4	PWMDnH3	PWMDnH2	PWMDnH1	PWMDnH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register PWMDnH (n=0-5) address: F141H, F143H, F145H, F147H, F149H, F14BH.

Bit7~ Bit0 PWMDnH<7:0>: PWM channel n is compare date(duty cycle data) high 8-bit register.

PWM Down Compare Data Low 8-bit Register (PWMDDnL)(n=0-5)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMDDnL	PWMDDnL7	PWMDDnL6	PWMDDnL5	PWMDDnL4	PWMDDnL3	PWMDDnL2	PWMDDnL1	PWMDDnL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register PWMDDnL (n=0-5) address: F150H, F152H, F154H, F156H, F158H, F15AH.

Bit7~ Bit0 PWMDDnL<7:0>: PWM channel n is down compare data low 8-bit register (duty cycle data in asymmetric counting).

PWM Down Compare Data High 8-bit Register (PWMDDnH) (n=0-5)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMDDnH	PWMDDnH7	PWMDDnH6	PWMDDnH5	PWMDDnH4	PWMDDnH3	PWMDDnH2	PWMDDnH1	PWMDDnH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register PWMDDnH (n=0-5) address: F151H, F153H, F155H, F157H, F159H, F15BH.

Bit7~ Bit0 PWMDDnH<7:0>: PWM channel n down compare data high 8-bit registers (duty cycle data in asymmetric counting).

PWM Dead Zone Enable Control Register (PWMDTE)

F160H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMDTE	--	--	--	--	--	PWM45DTE	PWM23DTE	PWM01DTE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit3 --

Bit2 PWM45DTE: Dead zone enable bit of PWM4/5 channel;
1= Enable;
0= Disable.

Bit1 PWM23DTE: Dead zone enable bit of PWM2/3 channel;
1= Enable;
0= Disable.

Bit0 PWM01DTE: Dead zone enable bit of PWM0/1 channel;
1= Enable;
0= Disable.

PWM 0/1 Dead Zone Delay Data Register (PWM01DT)

F161H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM01DT	PWM01DT7	PWM01DT6	PWM01DT5	PWM01DT4	PWM01DT3	PWM01DT2	PWM01DT1	PWM01DT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 PWM01DT<7:0>: PWM channel 0/1 is dead zone delay data register.

PWM 2/3 Dead Zone Delay Data Register (PWM23DT)

F162H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM23DT	PWM23DT7	PWM23DT6	PWM23DT5	PWM23DT4	PWM23DT3	PWM23DT2	PWM23DT1	PWM23DT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 PWM23DT<7:0>: PWM channel 2/3 is dead zone delay data register.

PWM4/5 Dead Zone Delay Data Register (PWM45DT)

F163H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM45DT	PWM45DT7	PWM45DT6	PWM45DT5	PWM45DT4	PWM45DT3	PWM45DT2	PWM45DT1	PWM45DT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 PWM45DT<7:0>: PWM channel 4/5 is dead zone delay data register.

PWM Mask Control Register (PWMMASKE)

F164H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMMASKE	--	--	PWM5MASKE	PWM4MASKE	PWM3MASKE	PWM2MASKE	PWM1MASKE	PWM0MASKE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit6 --

Bit5~Bit0 PWMnMASKE: PWM channel n mask control enable bit (n=0-5);

1= PWMn channel enable mask data output;

0= The PWMn channel disables mask data output (normal PWM waveform output).

PWM Mask Control Register (PWMMASKD)

F165H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMMASKD	--	--	PWM5MASKD	PWM4MASKD	PWM3MASKD	PWM2MASKD	PWM1MASKD	PWM0MASKD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit6 --

Bit5~Bit0 PWMnMASKD: PWM channel n mask data bits (n=0-5);

1= PWMn channel output high;

0= PWMn channel output is low.

PWM Brake Control Register (PWMFBKC)

F166H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMFBKC	PWMFBIE	PWMFBF	PWM5FBCCE	PWMFBKSW	PWMFBES	--	PWMFBEN	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 PWMFBIE: PWM's brake interrupt mask bit;
1= Enable interrupt;
0= Disable interrupt.
Bit6 PWMFBF: PWM's Brake mark (writing 0 is clear);
1= Enable (PWM output value of brake data register);
0= Disable.
Bit5 PWMFBCCE: Whether to clear all channel counter selection bits when PWM brakes;
1= Enable;
0= Disable.
Bit4 PWMFBKSW: PWM's Software brake signal start bit;
1= Enable;
0= Disable.
Bit3 PWMFBES: PWM's external hardware brake channel 1 (FB) trigger level select bit;
1= High level trigger;
0= Low level trigger
Bit2 -- Reserved, must be 0.
Bit1 PWMFBEN: PWM's external hardware brake channel 1 (FB) enable bit;
1= Enable;
0= Disable.
Bit0 -- Reserved, must be 0.

PWM Brake Data Register (PWMFBKD)

F167H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMFBKD	--	--	PWM5FBKD	PWM4FBKD	PWM3FBKD	PWM2FBKD	PWM1FBKD	PWM0FBKD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 Not used.
Bit5~Bit0 PWMnFBKD: PWM channel n brake data bit (n=0-5);
1= PWMn channel's output is high after brake operation.
0= PWMn channel's output is low after brake operation.

PWM Period Interrupt Mask Register (PWMPIE)

F168H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMPIE	--	--	PWM5PIE	PWM4PIE	PWM3PIE	PWM2PIE	PWM1PIE	PWM0PIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --

Bit5~Bit0 PWMnPIE: PWM channel n period interrupt mask bit (n=0-5)

1= Enable interrupt;

0= Disable interrupt.

PWM Zero Interrupt Mask Register (PWMZIE)

F169H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMZIE	--	--	PWM5ZIE	PWM4ZIE	PWM3ZIE	PWM2ZIE	PWM1ZIE	PWM0ZIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --

Bit5~Bit0 PWMnZIE: PWM channel n zero interrupt mask bit (n=0-5);

1= Enable interrupt;

0= Disable interrupt.

PWM Up Compare Interrupt Mask Register (PWMUIE)

F16BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMUIE	--	--	PWM5UIE	PWM4UIE	PWM3UIE	PWM2UIE	PWM1UIE	PWM0UIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --

Bit5~Bit0 PWMnUIE: PWM channel n up compare interrupt mask bit (n=0-5);

1= Enable interrupt;

0= Disable interrupt.

PWM Down Compare Interrupt Mask Register (PWMDIE)

F16BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMDIE	--	--	PWM5DIE	PWM4DIE	PWM3DIE	PWM2DIE	PWM1DIE	PWM0DIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --

Bit5~Bit0 PWMnDIE: PWM channel n down compare interrupt mask bit (n=0-5);

1= Enable interrupt;

0= Disable interrupt.

PWM Period Interrupt Flag Register (PWMPIF)

F16CH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMPIF	--	--	PWM5PIF	PWM4PIF	PWM3PIF	PWM2PIF	PWM1PIF	PWM0PIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --

Bit5~Bit0 PWMnPIF: PWM channel n period interrupt flag bit (n=0-5);

1= Generate an interrupt (software clear);

0= No interrupt.

PWM Zero Interrupt Flag Register (PWMZIF)

F16DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMZIF	--	--	PWM5ZIF	PWM4ZIF	PWM3ZIF	PWM2ZIF	PWM1ZIF	PWM0ZIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --

Bit5~Bit0 PWMnZIF: PWM channel n zero interrupt flag bit (n=0-5);

1= Generate an interrupt (software clear);

0= No interrupt.

PWM Up Compare Interrupt Flag Register (PWMUIF)

F16FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMUIF	--	--	PWM5UIF	PWM4UIF	PWM3UIF	PWM2UIF	PWM1UIF	PWM0UIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --

Bit5~Bit0 PWMnUIF: PWM channel n up compare interrupt flag bit (n=0-5);

1= Generate an interrupt (software clear);

0= No interrupt.

PWM Down Compare Interrupt Flag Register (PWMDIF)

F16FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMDIF	--	--	PWM5DIF	PWM4DIF	PWM3DIF	PWM2DIF	PWM1DIF	PWM0DIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit6 --

Bit5~Bit0 PWMnDIF: PWM channel n down compare interrupt flag bit (n=0-5);

1= Generate an interrupt (software clear);

0= No interrupt.

15. I²C MODULE

15.1 Overview

This model provides interface between microprocessor and I²C bus. The I²C supports arbitration and clock synchronization so that it can run in multi-master system. The I²C supports normal mode and fast mode.

The main features of the model include:

- Supports four transfer mode: master transmitter, master receiver, slave transmitter and slave receiver.
- Supports two transfer speed mode:
  - Standard speed(up to 100Kbs);
  - Fast speed (high to 400Kbs);
- Supports arbitration and clock synchronization.
- Supports multi-master system.
- Master mode supports 7-bit addressing mode and 10-bit addressing mode on I²C bus.
- Slave mode s supports 7-bit addressing mode on I²C bus.
- Generate interrupt.
- Operate at a wide range of clock frequency(8-bit internal timer).

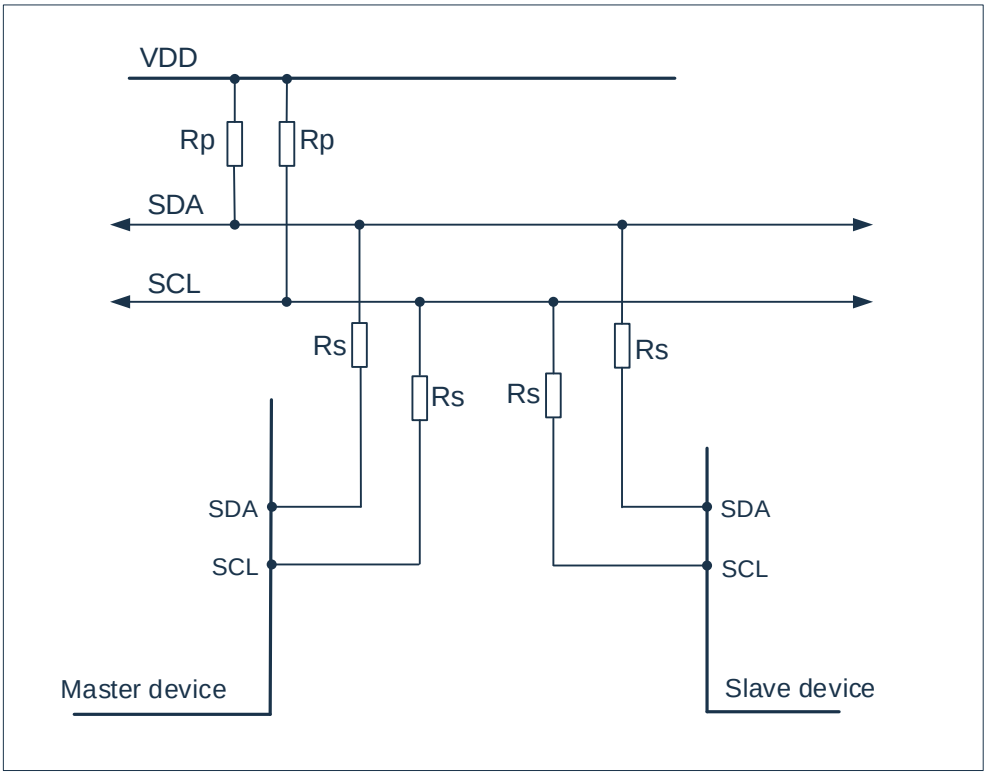


Figure15-1: I²C Interconnection

15.2 I²C Port Configuration

If you use the I²C function, you should first configure the corresponding ports as SCL, SDA channels (any GPIO can be configured as I²C channel). For example, to configure P0.4, P0.5 ports as I²C function.

```
P04CFG=0x0C.    // Select P0.4 to configure as SCL channel
P05CFG=0x0D.    // Select P0.5 configuration as SDA channel
```

After configuring the I²C channel, this group of ports is open-drain by default. You can configure whether to enable the internal pull-up resistors of SCL and SDA ports through PxUP, or add pull-up resistors outside the chip.

In master mode, the IIC outputs SCL to the slave. After sending address or data, the slave needs to pull down SCL and send back the corresponding response signal to the master. The master needs to read back the SCL port line status to detect whether the slave releases SCL to determine whether the next data frame needs to be sent. If the pull-up resistor or board-level parasitic capacitance of SCL is larger, it will lead to longer read-back time, which will affect the communication speed of IIC, please refer to the IIC application manual for details.

15.3 I²C Master Mode

The six register that is connected with host machine are as follows : control, status, address of slave machine, send data, receive data and period register.

Register		Address
Write	Read	
Slave address register I2CMSA	Slave address register I2CMSA	0xF4
Control register in master mode I2CMCR	Status register in master mode I2CMSR	0xF5
Transmit data register in master mode I2CMBUF	Receive data register in master mode I2CMBUF	0xF6
Period timing register I2CMTP	Period timing register I2CMTP	0xF7

In master mode, control register and status register use the same address, but they are physically different register.

In master mode, transmitting data register and receiving data register use the same register address,

Write operation access transmitting data register(I2CMBUF), Read operation access receiving data register(I2CMBUF).

Write operation is executed by control register. Read operation is executed by status register.

15.3.1 I²C Timing Period Register In Master Control Mode

To generate a wide range of SCL frequencies, the module has a built-in 8-bit timer. For standard and fast transmission.

Ideal clock period of SCL when TIMER_PRD ≠ 0: 2* (1+TIMER_PRD)* 10* Tsys

Ideal clock period of SCL when TIMER_PRD = 0: 3* 10* Tsys

Refer to the IIC application manual for the specific equations of SCL calculation.

0xF7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CMTP	--	MTP6	MTP5	MTP4	MTP3	MTP2	MTP1	MTP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	1

Bit7	Reserved:	It must be zero.
Bit6~ Bit0	MTP6-MTP0:	Bits 6-0 of the period timing register for standard and fast modes: TIMER_PRD[6:0].

15.3.2 I²C Master Mode Control and Status Register

The control register consists of 4 bits: RUN, START, STOP, ACK bits. The START bit will generate a START or REPEATED START condition. The STOP bit determines whether the data transfer will stop at the end of the cycle or continue it. To generate a single transmit cycle, the slave address register is written with the desired address, the R/S bit is set to 0 and the control register is written with ACK=x, STOP=1, START=1, RUN=1 (I2CMCR=xxx0_x111x) to perform the operation and stop. When the operation is completed (or an error occurs), an interrupt is generated. Data can be read from the receive data register.

When the I2 C is operating in master mode, the ACK bit must be set to 1. This will cause the I2 C bus controller to automatically send an answer after each byte. This bit must be cleared to 0 when the I2 C bus controller no longer needs the slave to send data.

Master Mode Control Register

0xF5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CMCR	RSTS	--	--	--	ACK	STOP	START	RUN
W	W	W	W	W	W	W	W	W
Reset value	0	0	0	0	0	0	0	0

Bit7 RSTS: I²C active module reset control bit;
1= Reset the master module (I² C registers of the entire master module, including I2CMSR);
0= I²C Interrupt flag bit cleared to 0 in master control mode.
Bit6~ Bit5 -- Disable accessing
Bit4 Reserved: Must to be 0.
Bit3 ACK: Response enable bit;
1= Enable;
0= Disable.
Bit2 STOP: Stop enable bit;
1= Enable;
0= Disable.
Bit1 START: Start enable bit;
1= Enable;
0= Disable.
Bit0 RUN: Run enable bit;
1= Enable;
0= Disable.

The combination of the following control bit list can realize all kinds of operations in master control module:

START: transmit start signal.

SEND: transmit data or address.

RECEIVE: receive data.

STOP: transmit end signal.

Combination of control bit (IDLE status)

R/S	ACK	STOP	START	RUN	OPERATION
0	-	0	1	1	START followed by SEND (master remains in transmit mode)
0	-	1	1	1	START followed by SEND and STOP
1	0	0	1	1	Non-response is used for reception after START (master remains in receiver mode)
1	0	1	1	1	START followed by RECEIVE and STOP
1	1	0	1	1	START followed by RECEIVE (master remains in receiver mode)
1	1	1	1	1	Disable combinations
0	0	0	0	1	Disable combinations

Combination of control bit (master send status)

R/S	ACK	STOP	START	RUN	OPERATION
-	-	0	0	1	SEND operation
-	-	1	0	0	Stop
-	-	1	0	1	SEND followed by STOP
0	-	0	1	1	Repeat START followed by SEND
0	-	1	1	1	Repeat START, followed by SEND and STOP
1	0	0	1	1	Repeat the START condition followed by the answer RECEIVE operation
1	0	1	1	1	(Master remains in receiver mode)
1	1	0	1	1	Repeat START, followed by SEND and STOP conditions
1	1	1	1	1	Repeat the START condition followed by RECEIVE

Combination of control bit (master receive status)

R/S	ACK	STOP	START	RUN	OPERATION
-	0	0	0	1	RECEIVE operation with answering
-	-	1	0	0	(Master remains in receiver mode)
-	0	1	0	1	STOP
-	1	0	0	1	RECEIVE followed by STOP
-	1	1	0	1	RECEIVE operation (master remains in receiver mode)
1	0	0	1	1	Disable combinations
1	0	1	1	1	Repeat START, followed by an answer RECEIVE operation
1	1	0	1	1	(Master remains in receiver mode)
0	-	0	1	1	Repeat START, followed by RECEIVE and STOP
0	-	1	1	1	Repeat START followed by RECEIVE

Status registers in master mode (I2CMSR)

0xF5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CMSR	I2CMIF	BUS_BUSY	IDLE	ARB_LOST	DATA_ACK	ADD_ACK	ERROR	BUSY
R	R	R	R	R	R	R	R	R
Reset value	0	0	1	0	0	0	0	0

Bit7 I2CMIF: Interrupt flag in I^2C master mode;
1= Complete send/receive in master mode, or occur transmit failure.
(Clear I2CMIF, need to write 0 to I2CMCR.RSTS);
0= No interrupt occurred.

Bit6 BUS_BUSY: The I^2C bus busy flag bit in master mode/salve mode;
1= The I^2C bus is working, that cannot transmit data
(this start bit of bus is set to 1 and the stop condition is set to 0)
0= ---

Bit5 IDLE: Idle flag in I^2C master mode;
1= Idle;
0= Work.

Bit4 ARB_LOST: Arbitration flag in I^2C master mode;
1= Lose control of bus.
0= ---

Bit3 DATA_ACK: The response of sending data in I^2C master control mode;
1= No response of the last sending data.
0= ---

Bit2 ADD_ACK: Addressing flag in I^2C master control mode;
1= No response of the last addressing.
0= ---

Bit1 ERROR: Failure flag in I^2C master control mode;
1= No response of addressing slave machine and arbitration conflict.
0= ---

Bit0 BUSY: Busy flag in I^2C master control mode;
1= Sending data.
0= ---

15.3.3 I²C Slave Address Register

The slave address register consists of 8 bits: 7 address bits (A6-A0) and receive/non-transmit bits R/S. The R/S bits determine whether the next operation is receive (1) or transmit (0).

Master Mode Slave Address Register (I2CMSA)

0xF4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CMSA	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/S
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit1 SA6-SA0: I²C Slave address in master mode.

Bit0 R/S: I²C Receive/send status selection bit after sending the slave address in master mode;

1= Receiving data after correct addressing;

0= Send data after correct addressing.

15.3.4 I²C Master Mode Transmit and Receive Data Register

The transmit data register consists of eight data bits that will be sent on the bus on the next transmit or burst transmit operation, and the first transmission bit is MD7 (MSB).

Master mode data cache register (I2CMBUF)

0xF6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CMBUF	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 MD7-MD0: I²C transmit/receive data in master mode.

15.4 I²C Slave Mode

There are five registers that is used to connect object device: address, control, send data and receive data.

Register		Address
Write	Read	
Self-address register I2CSADR	Self-address register I2CSADR	0xF1
Control register I2CSCR	Status register I2CSSR	0xF2
Send data I2CSBUF	Receive data I2CSBUF	0xF3

15.4.1 I²C Own Address Register I2CSADR

The own address register is made up of 7 bits that identify the I2C core on the I2C bus. This register can read and write addresses.

Own Address Register (I2CSADR)

0xF1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CSADR	--	SA6	SA5	SA4	SA3	SA2	SA1	SA0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 --

Bit6~Bit0 SA6-SA0: Own address in I²C salve mode.

15.4.2 I²C Slave Mode Control and Status Register I2CSCR/I2CSSR

In slave mode, control register and status register occupy a register address and use different operations to distinguish access to the two registers.

Write: write I2CSCR (write only)

Read: read I2CSSR (read only)

The control register consists of two bits: RSTS and DA. The RSTS controls the reset of the entire I2C salve module. When the I2C encounters some problems, the I2CS can be reinitialized by using RSTS. The DA can enable and disable I2CS device. Read the address place the status register on the data bus.

Slave Mode Control Register (I2CSCR)

0xF2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CSCR	RSTS	--	--	--	--	--	--	DA
R/W	W	R	R	R	R	R	R	W
Reset value	0	0	0	0	0	0	0	0

Bit7 RSTS: Reset control bit in I²C slave mode;
1= Reset slave module;
0= No effect.

Bit6~ Bit1 --

Bit0 DA: Enable bit in I²C slave mode;
1= Enable;
0= Disable.

The status register consists of three bits: the SENDFIN bit, the RREQ bit, and the TREQ bit. The Send Complete SENDFIN bit indicates that the host I²C controller has completed receiving data during an I2CS single or continuous transmit operation. The Receive Request RREQ bit indicates that the I2CS device has received a data byte from the I²C host and that the I2CS device should read a data byte from the Receive Data Register I2CSBUF. The Transmit Request TREQ bit indicates that the I2CS device is addressed as a slave transmitter and the I2CS device shall write a data byte to the transmit data register I2CSBUF. If the I²C interrupt enable is on, an interrupt is generated by setting any of the three flag bits to 1.

The bus busy flag bit in slave mode is judged by Bit6 (BUS_BUSY) of I2CMSR in master mode status register. I2CMSR is 0x20 when the bus is idle, and I2CMSR register is 0x60 when the start condition is generated until the stop condition is generated.

Slave Mode Status Register (I2CSSR)

0xF2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CSSR	--	--	--	--	--	SENDFIN	TREQ	RREQ
R/W	--	--	--	--	--	R	R	R
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit3 --

Bit2 SENDFIN: Sending complete flag bit In I²C slave mode (read only).

1= The master control device no longer needs data, the TREQ is no longer set to 1, and the data transmission has been completed.(automatically cleared after reading I2CSCR)

0= ---

Bit1 TREQ: Prepared sending flag bit In I²C slave mode (read only).

1= The master control device is ready to receive data.
(automatically write zero after writing I2CSBUF)

0= ---

Bit0 RREQ: Receiving complete flag bit In I²C slave mode (read only).

1= Receive complete. (automatically write zero after reading I2CSBUF)

0= Receive uncompleted.

15.4.3 I²C Slave Mode Transmit and Receive Buffer Register (I2CSBUF)

0xF3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CSBUF	I2CSBUF7	I2CSBUF6	I2CSBUF5	I2CSBUF4	I2CSBUF3	I2CSBUF2	I2CSBUF1	I2CSBUF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit0 I2CSBUF: I²C Sending/receiving data.

Write: Send data (Send order from MSB to LSB).

Read: Read received dates.

15.5 I²C Interrupt

The interrupt number of I²C is 21, where the interrupt vector is 0x00AB. To enable I²C interrupt, the enable bit(I2CIE) is set to 1, and the master interrupt enable bit(EA) is set to 1.

If all the interrupt enable is turned on and master interrupt enable(I2CIF) is set to 1,then the CPU will enter the interrupt service program. The I2CIF property is read-only and has nothing to do with the state of I2CIE.

Interrupt flag bit (I2CMIF) in master mode, SENDFIN in slave mode, TREQ in slave mode and RREQ in slave mode, when any one of them is 1, the master interrupt flag bit (I2CIF) of I²C is set to 1. When the 4 flag bits are all 0, the I2CIF will automatically clear 1.

Interrupt Mask Register (EIE2)

0xAA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIE2	SPIIE	I2CIE	WDTIE	ADCIE	PWMIE	--	ET4	ET3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPIIE: SPI Interrupt enable bit
1= Enable SPI interrupt;
0= Disable SPI interrupt.
Bit6 I2CIE: I²C Interrupt enable bit
1= Enable I²C interrupt;
0= Disable I²C interrupt.
Bit5 WDTIE: WDT Interrupt enable bit
1= Enable WDT interrupt;
0= Disable WDT interrupt.
Bit4 ADCIE: ADC Interrupt enable bit
1= Enable ADC interrupt;
0= Disable ADC interrupt.
Bit3 PWMIE: PWM global interrupt enable bit
1= Enable PWM global interrupt;
0= Disable PWM global interrupt.
Bit2 --
Bit1 ET4: Time4 Interrupt enable bit
1= Enable Time4 interrupt;
0= Disable Time4 interrupt.
Bit0 ET3: Time3 Interrupt enable bit
1= Enable Time3 interrupt;
0= Disable Time3 interrupt.

Peripheral Interrupt Priority Control Register (EIP2)

0xBA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIP2	PSPI	PI2C	PWDT	PADC	PPWM	--	PT4	PT3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 PSPI: SPI interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit6 PI2C: I^2C interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit5 PWDT: WDT interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit4 PADC: ADC interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit3 PPWM: PWM interrupt priority control bit
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit2 --

Bit1 PT4: TIMER4 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit0 PT3: TIMER3 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Peripheral Interrupt Flag Register (EIF2)(0xB2)

0xB2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIF2	SPIIF	I2CIF	--	ADCIF	PWMIF	--	TF4	TF3
R/W	R	R	--	R/W	R	--	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPIIF: SPI bus interrupt instruction, Read only;
1= SPI interrupt, (Automatically cleared after clearing the specific interrupt flag);
0= No SPI interrupt.
Bit6 I2CIF: I^2C Total interrupt instruction, Read only;
1= I^2C interrupt, (Automatically cleared after clearing the specific interrupt flag);
0= No I^2C interrupt.
Bit5 --
Bit4 ADCIF: ADC interrupt flag;
1= ADC Conversion completed, need software clear;
0= ADC conversion is not complete.
Bit3 PWMIF: PWM Total interrupt instruction, Read only;
1= PWM interrupt, (Automatically cleared after clearing the specific interrupt flag);
0= No PWM interrupt.
Bit2 --
Bit1 TF4: Timer4 timer overflow interrupt flag;
1= Timer4 enter the interrupt service routine, the hardware automatically clears, or can be cleared by software;
0= Timer4 timer has no overflow.
Bit0 TF3: Timer3 timer overflow interrupt flag;
1= Timer3 enter the interrupt service routine, the hardware automatically clears, or can be cleared by software;
0= Timer3 timer has no overflow.

15.6 I²C Transmission Mode In Slave Mode

This section describes all available transmission mode in the kernel. The default address of all the waveform is 0x39(“00111001”).

15.6.1 Single Receiving

The following figure shows the sequence of signals received by I2C during single data. Single receiving sequence is as follows:

- Starting conditions.
- Addressing by I²C master.
- The address is confirmed by I2C.
- The data is received by I²C.
- The data is confirmed by I²C.
- Stop conditions.

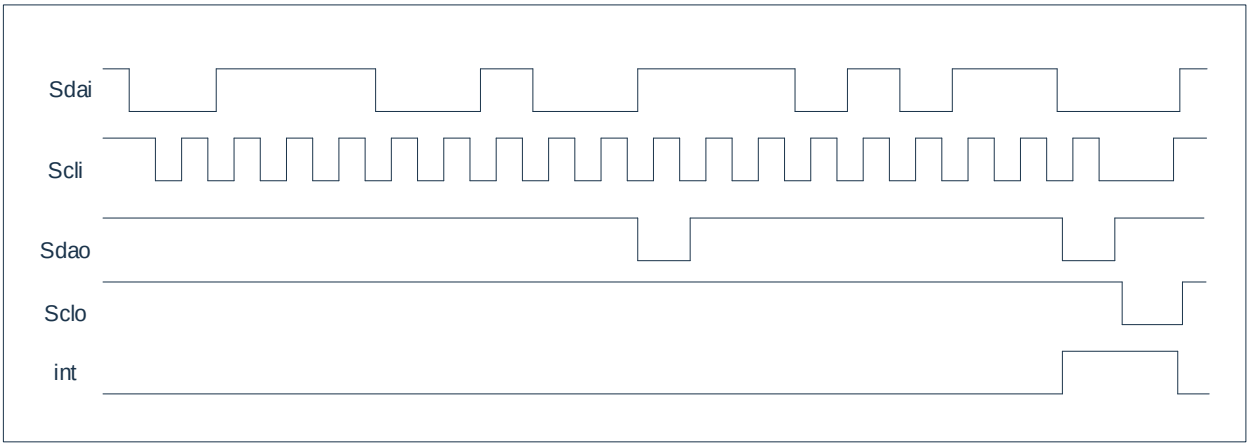


Figure 15-2: Timing diagram of single receiving

15.6.2 Single Sending

The following figure shows the sequence of signals sent by I2C during a single data period. Single transmission sequence:

- Starting conditions.
- Addressing by I^2C master.
- The address is confirmed by I^2C.
- The data is transmitted by I^2C.
- The data is not confirmed by I^2C.
- Stop conditions.

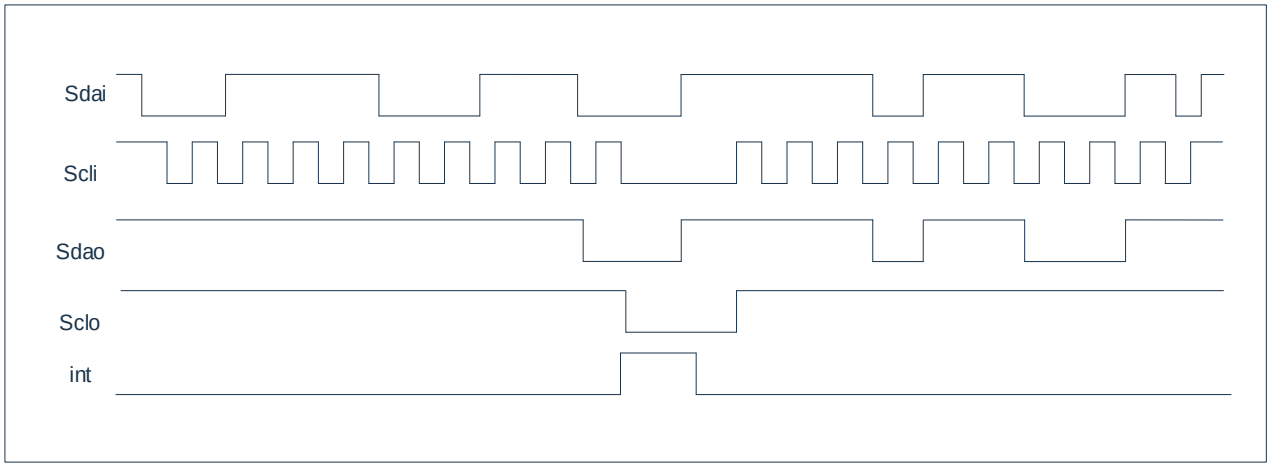


Figure 15-3: Timing diagram of single sending

15.6.3 Continuous Receiving

The following figure shows the sequence of signals received by I²C during burst data. Burst receiving sequence is as follows:

- Starting conditions.
- Addressing by I²C master.
- The address is confirmed by I²C.
  (1) The data is received by I²C.
  (2) The data is confirmed by I²C.
- Stop conditions.

Repeat sequence (1) and sequence (2) until the stop condition occurs.

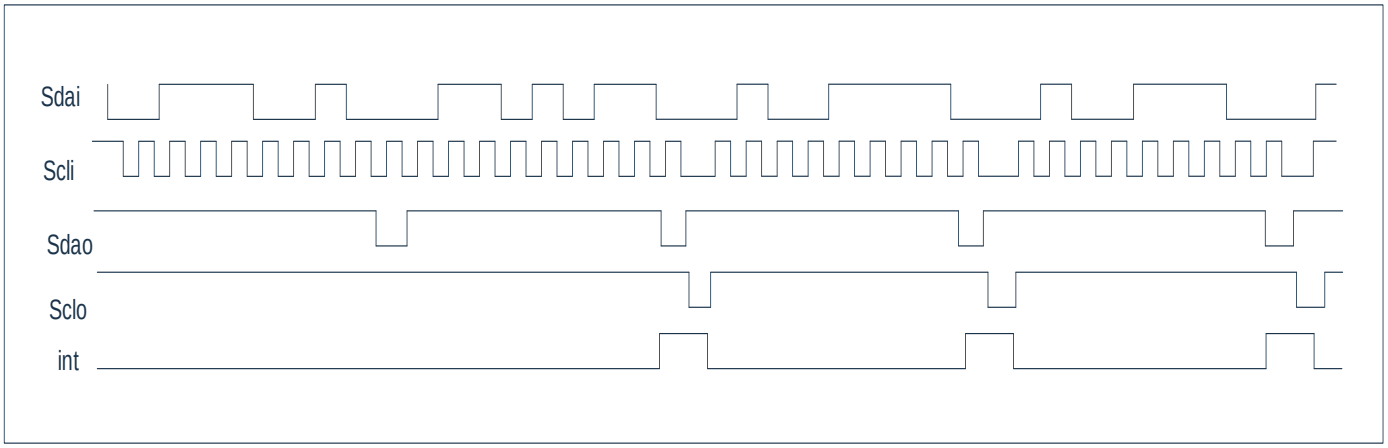


Figure 15-4: Timing diagram of continuous receiving

15.6.4 Continuous Sending

The following figure shows the sequence of signals sended by I²C during burst data. Burst sending sequence is as follows:

- Starting conditions.
- Addressing by I²C master.
- The address is confirmed by I²C.
  (1) The data is sended by I²C.
  (2) The data is confirmed by I2C.
  (3) The last data is not confirmed by I²C.
- Stop conditions.

Repeat sequence (1) and sequence (2) until sequence (3) occurs.

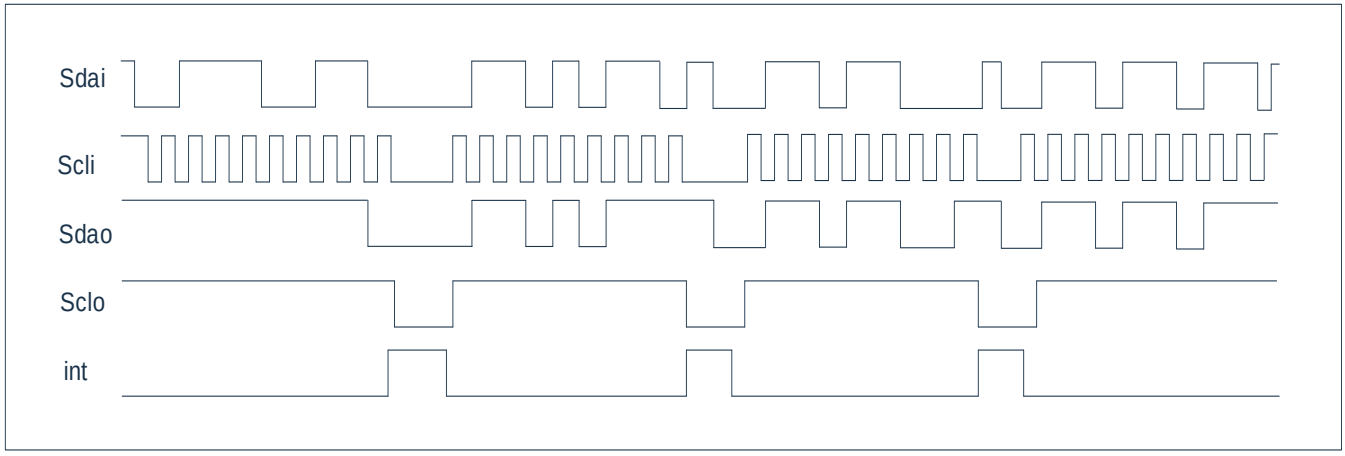


Figure 15-5: Timing diagram of continuous sending

16. BRT MODULE

16.1 Introduction

There is a 16-bit baut-rate timer inside the chip, which mainly provides the clock for the UART module.

16.2 Function Description

BRT has one 16-bit counter internally. The initial value of the counter is loaded by {BRTDH, BRTDL}, and the counter starts to operate when BRTEN=1. Its clock comes from the prescaler circuit, and the prescaler clock is determined by BRTCKDIV.

The counter works as an incremental counter, and the BRT counter overflows when the value of the 16-bit counter is equal to FFFFH. The value of {BRTDH, BRTDL} is automatically loaded into the counter after the overflow, and then the counting is done again.

The overflow signal of the BRT counter is provided exclusively to the UART module as a clock source for the baud rate. No interrupts are generated on overflow. There is also no corresponding interrupt structure.

When BRT is in debug mode, its clock will not stop. If the UART module has started to send or receive data, the UART will complete the whole process of sending or receiving even if the chip goes into stop state.

BRT timer overflow rate:

$$BRTov=\frac{Fsys}{(65536-\{BRTDH,BRTDL\})\times 2^{BRTCKDIV}}$$

16.3 Register Description

BRTCON Register

F5C0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BRTCON	BRTEN	--	--	--	--	BRTCKDIV2	BRTCKDIV1	BRTCKDIV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

BRTEN: BRT timer enable bit;

Bit7 1= Enable;

0= Disable.

Bit6~ Bit3 --

Bit2~Bit0 BRTCKDIV<2:0> BRT timer prescaler selection bit;

000= Fsys/1;

001= Fsys/2;

010= Fsys/4;

011= Fsys/8;

100= Fsys/16;

101= Fsys/32;

110= Fsys/64;

111= Fsys/128.

BRTDL Register

F5C1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BRTDL	BRTDL7	BRTDL6	BRTDL5	BRTDL4	BRTDL3	BRTDL2	BRTDL1	BRTDL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 BRTDL<7:0>: Lower 8 bits of the BRT timer load value;

BRTDH Register

F5C2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BRTDH	BRTDH7	BRTDH6	BRTDH5	BRTDH4	BRTDH3	BRTDH2	BRTDH1	BRTDH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 BRTDH<7:0>: Higher 8 bits of the BRT timer load value;

The following table gives some of the baud rate related information for the baud rate timer overflow rate as the UART clock source in variable baud rate mode:

SMODn=0, BRTCKDIV=0

	Fsys=8MHz			Fsys=16MHz			Fsys=24MHz			Fsys=48MHz		
	{BRTH, BRTL}	Actual Rate	% Error	{BRTH, BRTL}	Actual Rate	% Error	{BRTH, BRTL}	Actual Rate	% Error	{BRTH, BRTL}	Actual Rate	% Error
4800	65484	4808	-0.16	65432	4808	-0.16	65380	4808	-0.16	65224	4808	-0.16
9600	65510	9615	-0.16	65484	9615	-0.16	65458	9615	-0.16	65380	9615	-0.16
19200	65523	19231	-0.16	65510	19231	-0.16	65497	19231	-0.16	65458	19231	-0.16
38400	--	--	--	65523	38462	-0.16	65516	37500	2.34	65497	38462	-0.16
115200	--	--	--	--	--	--	--	--	--	65523	115385	-0.16
250000	--	--	--	--	--	--	--	--	--	65530	250000	0
500000	--	--	--	--	--	--	--	--	--	65533	500000	0

SMODn=1, BRTCKDIV=0

	Fsys=8MHz			Fsys=16MHz			Fsys=24MHz			Fsys=48MHz		
	{BRTH, BRTL}	Actual Rate	% Error	{BRTH, BRTL}	Actual Rate	% Error	{BRTH, BRTL}	Actual Rate	% Error	{BRTH, BRTL}	Actual Rate	% Error
4800	65432	4808	-0.16	65328	4808	-0.16	65224	4792	0.16	64911	4800	0
9600	65484	9615	-0.16	65432	9615	-0.16	65380	9615	-0.16	65224	9615	-0.16
19200	65510	19231	-0.16	65484	19231	-0.16	65458	19231	-0.16	65380	19231	-0.16
38400	65523	38462	-0.16	65510	38462	-0.16	65497	38462	-0.16	65458	38462	-0.16
115200	--	--	--	--	--	--	65523	115385	-0.16	65510	115385	-0.16
250000	--	--	--	--	--	--	--	--	--	65524	250000	0
500000	--	--	--	--	--	--	--	--	--	65530	500000	0
1000000	--	--	--	--	--	--	--	--	--	65533	1000000	0

17. UARTn MODULE (n=0,1)

17.1 Introduction

There are 2 UART modules included in the chip: UART0 and UART1,they have identical functions.

The serial port is full duplex, which means it can transmit and receive synchronously. Receive module is double-buffered, which means it can start to receive a second byte before a previously received byte has been read from the receive register. Data are loaded to transmit register by writing SBUFn register, and it could access a receive register with independent physical addresses by reading SBUFn register.

The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and 3 has special features for multi-processor communications. This feature is enabled by setting SMn2 bit in SCONn register. The master firstly sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. When SMn2 = 1, slave will not be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SMn2 bit and prepare to receive the data bytes that will be coming. The slaves that were not being addressed will set “1” to SMn2 bit and ignore the incoming data.

17.2 UARTn Port Configuration

Before using the UARTn module, you need to configure the corresponding ports as UARTn TXDn and RXDn channels (any GPIO can be configured as UARTn channel), for example:

P25CFG = 0x08;// P2.5 is configured as TXD0 channel

P26CFG =0x09;// P2.6 is configured as RXD0 channel, this port is automatically configured as open drain output with pull-up register when using master synchronous mode.

P35CFG = 0x0A;// P3.5 is configured as TXD1 channel

P21CFG =0x0B;/ P2.1 is configured as RXD1 channel, this port is automatically configured as open drain output with pull-up register when using master synchronous mode. Suggested that it sets up work mode firstly, then to configure related ports as serial port.

17.3 UARTn Baud Rate

In mode 0, the baud rate is fixed at twelve divisions of the system clock (Fsys/12); in mode 2, the baud rate is fixed at thirty-two divisions of the system clock or sixty-four divisions (Fsys/32, Fsys/64); in modes 1 and 3, the baud rate is generated by Timer1 or Timer4 or Timer2 or BRT module, and the choice of timer as the baud rate clock source is determined by register FUNCCR.

When {FUNCCR[2],FUNCCR[0]}=00, Timer1 is selected as the baud rate generator of UART0;
When {FUNCCR[2],FUNCCR[0]}=01, Timer4 is selected as the baud rate generator of UART0;
When {FUNCCR[2],FUNCCR[0]}=10, Timer2 is selected as the baud rate generator of UART0;
When {FUNCCR[2],FUNCCR[0]}=11, BRT is selected as the baud rate generator of UART0.
When {FUNCCR[3],FUNCCR[1]}=00, Timer1 is selected as the baud rate generator of UART1;
When {FUNCCR[3],FUNCCR[1]}=01, Timer4 is selected as the baud rate generator of UART1;
When {FUNCCR[3],FUNCCR[1]}=10, Timer2 is selected as the baud rate generator of UART1;
When {FUNCCR[3],FUNCCR[1]}=11, BRT is selected as the baud rate generator of UART1.

Equation for baud rate for Timer1 or Timer4 operating in 8-bit auto-reload mode:

$$BaudRate=\frac{Fsys\times 2^{SMODn}}{32\times(4\times 3^{1-TxM})\times(256-THx)}(x=1,4)$$

SMODn is the baud rate selection bit, set by register PCON. T1M is the Timer1 clock selection bit, set by register CKCON[4], and T4M is the Timer4 clock selection bit, set by register T34MOD[6]. That is, the value of TH1/TH4 for Timer1 or Timer4 at the corresponding baud rate should be set as follow:

$$THx=256-\frac{Fsys\times 2^{SMODn}}{32\times(4\times 3^{1-TxM})\times BaudRate}(x=1,4)$$

Equation for baud rate for Timer2 operating in overflow auto-reload mode:

$$BaudRate=\frac{Fsys\times 2^{SMODn}}{32\times(12\times 2^{T2PS})\times(65536-\{RLDH,RLDL\})}$$

T2PS is Timer2 clock prescaler selection bit, set by register T2CON[7]. That is, the value of Timer2 at the corresponding baud rate{RLDH,RLDL}should be set to:

$$\{RLDH,RLDL\}=65536-\frac{Fsys\times 2^{SMODn}}{32\times(12\times 2^{T2PS})\times BaudRate}$$

When BRT is used as a baud rate generator, the baud rate formula:

$$BaudRate=\frac{Fsys\times 2^{SMODn}}{32\times(65536-\{BRTDH,BRTDL\})\times 2^{BRTCKDIV}}$$

BRTCKDIV is the BRT timer prescaler selection bit, which is set by register BRTCON. That is, the BRT at the corresponding baud rate {BRTDH,BRTDL}value should be set as follows:

$$\{BRTDH,BRTDL\}=65536-\frac{Fsys\times 2^{SMODn}}{32\times 2^{BRTCKDIV}\times BaudRate}$$

The following table shows the related information of partial baud rate for Timer1/Timer4 8-bit auto-reload mode under variable baud rate mode:

SMODn=0

	Fsys=8MHz				Fsys=16MHz				Fsys=24MHz				Fsys=48MHz			
	TH1 or TH4	T1M or T4M	Actual Rate	% Error	TH1 or TH4	T1M or T4M	Actual Rate	% Error	TH1 or TH4	T1M or T4M	Actual Rate	% Error	TH1 or TH4	T1M or T4M	Actual Rate	% Error
4800	243	1	4808	-0.16	230	1	4808	-0.16	217	1	4808	-0.16	178	1	4808	-0.16
9600	--	--	--	--	247	1	9615	-0.16	236	1	9375	2.34	217	1	9615	-0.16
19200	--	--	--	--	--	--	--	--	246	1	18750	2.34	236	1	18750	2.34
38400	--	--	--	--	--	--	--	--	251	1	37500	2.34	246	1	37500	2.34

SMODn=1

	Fsys=8MHz				Fsys=16MHz				Fsys=24MHz				Fsys=48MHz			
	TH1 or TH4	T1M or T4M	Actual Rate	% Error	TH1 or TH4	T1M or T4M	Actual Rate	% Error	TH1 or TH4	T1M or T4M	Actual Rate	% Error	TH1 or TH4	T1M or T4M	Actual Rate	% Error
4800	230	1	4808	-0.16	204	1	4808	-0.16	178	1	4808	-0.16	100	1	4808	-0.16
9600	243	1	9615	-0.16	230	1	9615	-0.16	217	1	9615	-0.16	178	1	9615	-0.16
19200	--	--	--	--	243	1	19230	-0.16	236	1	18750	2.34	217	1	19231	-0.16
38400	--	--	--	--	--	--	--	--	246	1	37500	2.34	236	1	37500	2.34

17.4 UARTn Register

The UARTn has the same functionality as a standard 8051 UART. The UART0 related registers are: SBUFn, SCONn, PCON(0x87), IE(0xA8) and IP(0xB8). The UARTn data buffer (SBUFn) consists of two separateregisters: transmit and receive registers. A data written into the SBUFn will be set in UARTn output register and startsa transmission. Reading SBUFn will read data from the UARTn receive register.

SCON0 register support bit addressing operation, but SCON1 register doesn't support this function. It should be paid attention when using assembly language.

UART Buffer Register (SBUFn)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUFn	BUFFERn7	BUFFERn6	BUFFERn5	BUFFERn4	BUFFERn3	BUFFERn2	BUFFERn1	BUFFERn0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	X	X	X	X	X	X	X	X

SBUF register address: 0x99; SBUF1 register address: 0xEB;

Bit7~Bit0 BUFFERn<7:0>: Data buffer register.
Write: UARTn starts to transmit data.
Read: Read received data.

UART Control Register (SCONn)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONn	UnSM0	UnSM1	UnSM2	UnREN	UnTB8	UnRB8	TIn	RIn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

SCON0 register address: 0x98; SCON1 register address: 0xEA.

Bit7~Bit6 UnSM0- UnSM1: Control bit for multi-processor communications;
00= Master synchronous mode;
01= 8-bit asynchronous mode, baud rate is variable;
10= 9-bit asynchronous mode, baud rate is Fsys/32 or Fsys/64;
11= 9-bit asynchronous mode, baud rate is variable.

Bit5 UnSM2: Enable bit for multi-processor communications;
1= Enable;
0= Disable.

Bit4 UnREN: Receive enable bit;
1= Enable;
0= Disable.

Bit3 UnTB8: The 9th bit of transmitting data, mainly used for transmitting of 9-bit asynchronous mode;
1= The 9th bit is 1;
0= The 9th bit is 0.

Bit2 UnRB8: The 9th bit of receiving data, mainly used for receiving of 9-bit asynchronous mode;
1= The 9th bit of receiving data is 1;
0= The 9th bit of receiving data is 0.

Bit1 TIn: Transmit interrupt flag (needs software clear);
1= Transmit buffer is empty, it can transmit next data.
0= ---

Bit0 RIn: Receive interrupt flag (needs software clear);
1= Receive buffer is full, it could read data from receive register.
0= ---

UARTn mode is listed in the table below:

SMn0	SMn1	Mode	Description	Baud rate
0	0	0	Shift register	Fsys/12
0	1	1	8-Bit UART	variable
1	0	2	9-Bit UART	Fsys/32 or /64
1	1	3	9-Bit UART	variable

UARTn baud rate

Mode	Baud rate
Mode0	Fsys/12
Mode1, 3	Controlled by Timer4/Timer1/Timer2/BRT, see section 16.3.
Mode2	SMODn=0: Fsys/64 SMODn=1: Fsys/32

SMODn bit is in the power management control register PCON register:

0x87	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD0	SMOD1	--	--	--	SWE	STOP	IDLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SMOD0: The UART0 baud rate multiplier bit;
1= Doubling the UART0 baud rate;
0= UART0 baud rate is normal.
Bit6 SMOD1: UART1 baud rate multiplier bit;
1= Doubling the UART1 baud rate;
0= UART1 baud rate is normal.
Bit5 --
Bit4~Bit3 Reserved bit: It must be 0.
Bit2 SWE: STOP status function wake-up enable bit;
(The system can be restarted by a power-down reset or an enabled external reset, regardless of the SWE value)
0= Disable of functional wake-up calls;
1= Enable function wake-up (can be woken up by external interrupt and timed wake-up)
Bit1 STOP: The dormant state control bit;
1= Entering the sleep state (automatically cleared by exiting STOP mode);
0= Not in the dormant state.
Bit0 IDLE: Idle status control bit;
1= Entering the idle state (automatically cleared when exiting IDLE mode);
0= Not in idle state.

17.5 UARTn Interrupt

The interrupt number of UART0 is 4 and its interrupt vector is 0x0023. The interrupt number of UART1 is 6 and its interrupt vector is 0x0033. To enable the UARTn interrupt, you must set its enable bit ESn to 1 and set the total interrupt enable bit EA to 1.

If the interrupt enable of UARTn is on and TIn=1 or RIn=1, the CPU will enter the corresponding interrupt service program. TIn/RIn is not related to the status of ESn. And it needs to be cleared by software.

Interrupt Mask Register (IE)

0xA8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 EA: Overall interrupt enable bit;
1= Enable all un-masked interrupt;
0= Disable all interrupt.

Bit6 ES1: UART1 interrupt enable bit;
1= Enable UART1 interrupt;
0= Disable UART1 interrupt.

Bit5 ET2: TIMER2 interrupt enable bit;
1= Enable TIMER2 interrupt;
0= Disable TIMER2 interrupt.

Bit4 ES0: UART0 interrupt enable bit;
1= Enable UART0 interrupt;
0= Disable UART0 interrupt.

Bit3 ET1: TIMER1 interrupt enable bit;
1= Enable TIMER1 interrupt;
0= Disable TIMER1 interrupt.

Bit2 EX1: External interrupt 1 enable bit;
1= Enable external interrupt 1;
0= Disable external interrupt 1.

Bit1 ET0: TIMER0 interrupt enable bit;
1= Enable TIMER0 interrupt;
0= Disable TIMER0 interrupt.

Bit0 EX0: External interrupt 0 enable bit;
1= Enable external interrupt 0;
0= Disable external interrupt 0.

Interrupt Priority Control Register (IP)

0xB8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IP	--	PS1	PT2	PS0	PT1	PX1	PT0	PX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 --

Bit6 PS1: UART1 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt;

Bit5 PT2: TIMER2 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit4 PS0: UART0 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit3 PT1: TIMER1 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit2 PX1: External interrupt 1 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit1 PT0: TIMER0 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit0 PX0: External interrupt 0 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

UART Control Register (SCONn)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCONn	SMn0	SMn1	SMn2	RENn	TBn8	RBn8	TIn	RIn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Register SCON0 address:0x98;Register SCON1 address:0xEA.

Bit7~Bit6	SMn0-SMn1:	Control bit for multi-processor communications;
	00=	Master synchronous mode;
	01=	8-bit asynchronous mode, baud rate is variable;
	10=	9-bit asynchronous mode, baud rate is Fsys/32 or Fsys/64;
	11=	9-bit asynchronous mode, baud rate is variable.
Bit5	SMn2:	Enable bit for multi-processor communications;
	1=	Enable;
	0=	Disable.
Bit4	RENn:	Receive enable bit;
	1=	Enable;
	0=	Disable.
Bit3	TBn8:	The 9th bit of transmitting data, mainly used for transmitting of 9-bit asynchronous mode;
	1=	The 9th bit is 1;
	0=	The 9th bit is 0.
Bit2	RBn8:	The 9th bit of receiving data, mainly used for receiving of 9-bit asynchronous mode;
	1=	The 9th bit of receiving data is 1;
	0=	The 9th bit of receiving data is 0.
Bit1	Tin:	Transmit interrupt flag (needs software clear);
	1=	Transmit buffer is empty, it can transmit next data.
	0=	---
Bit0	RIn:	Receive interrupt flag (needs software clear);
	1=	Receive buffer is full, it could read data from receive register.
	0=	---

17.6 UARTn Mode (n=0/1)

17.6.1 Mode 0 - Synchronous Mode

Pin RXDn serves as input and TXDn as output. TXDn output is a shift clock. The baud rate is fixed at 1/12 of the CLK clock frequency. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON0 as follows: RIn=0 and RENn=1.

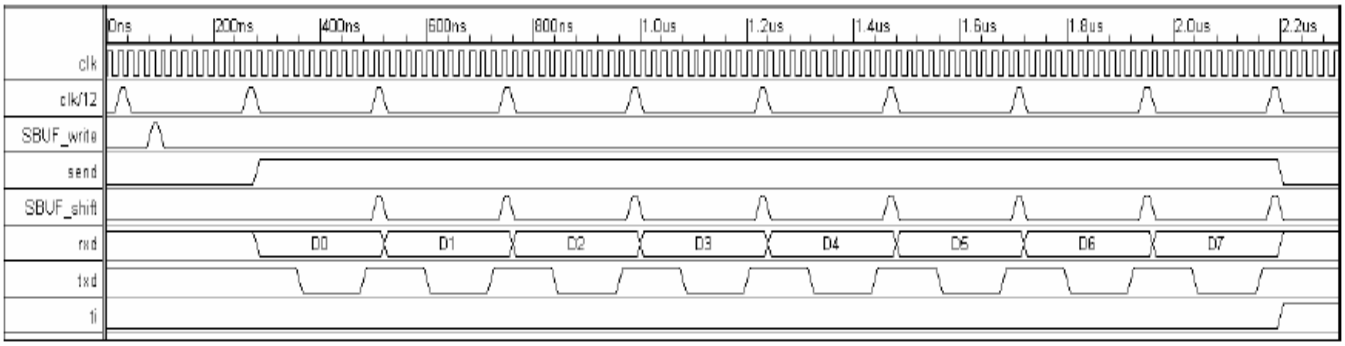


Figure 17-1: UARTn communication mode 0 timing diagram

17.6.2 Mode 1- 8-Bit Asynchronous Mode (Variable Baud Rate)

Pin RXDn serves as input, and TXDn serves as serial output. 10 bits are transmitted: a start bit (always 0), 8 data bits(LSB first), and a stop bit (always 1). When receive, a start bit synchronizes the transmission, 8 data bits are got by reading SBUFn, and stop bit sets the flag RBn8 in the register: SCONn. The baud rate is variable and depends on the mode of TIMER1, TIMER2, TIMER4 or BRT mode.

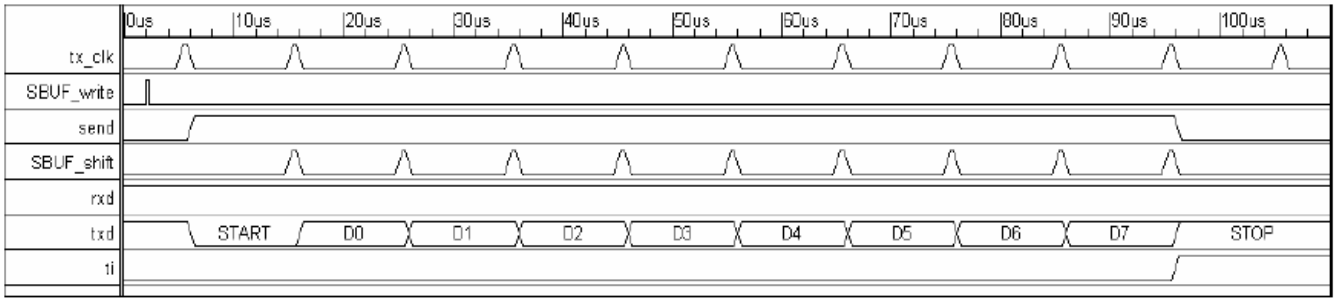


Figure 17-2: UARTn communication mode 1 timing diagram

17.6.3 Mode 2 - 9-Bit Asynchronous Mode (Fixed Baud Rate)

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of CLK clock frequency, and11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The9th bit can be used to control the parity checking of the UARTn interface: at transmission, bit TBn8 in SCONn is output as the 9thbit, and at receive, the 9th bit affects RBn8 in SCONn.

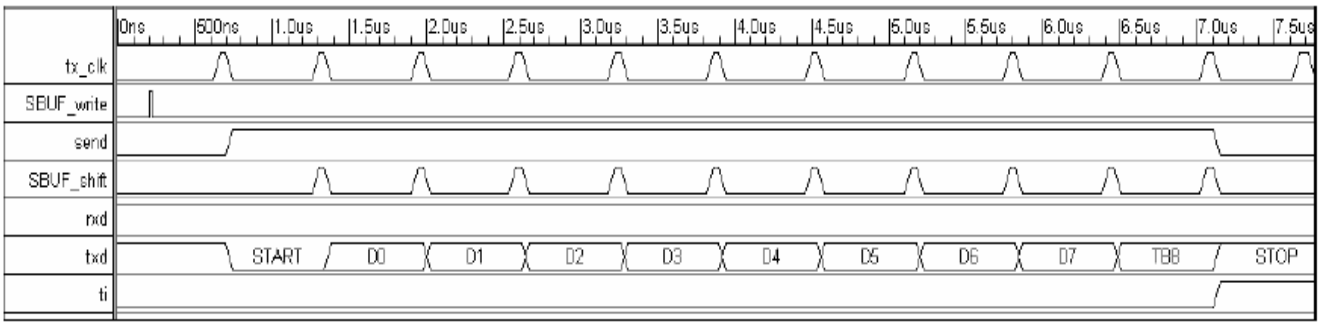


Figure 17-3: UARTn communication mode 2 timing diagram

17.6.4 Mode 3 - 9-Bit Asynchronous Mode (Variable Baud Rate)

The only difference between Mode 2 and Mode 3 is that the baud rate is variable in Mode 3. When REN0=1,datareceiving is enabled. The baud rate is variable and depends on the mode of TIMER1 or TIMER4.

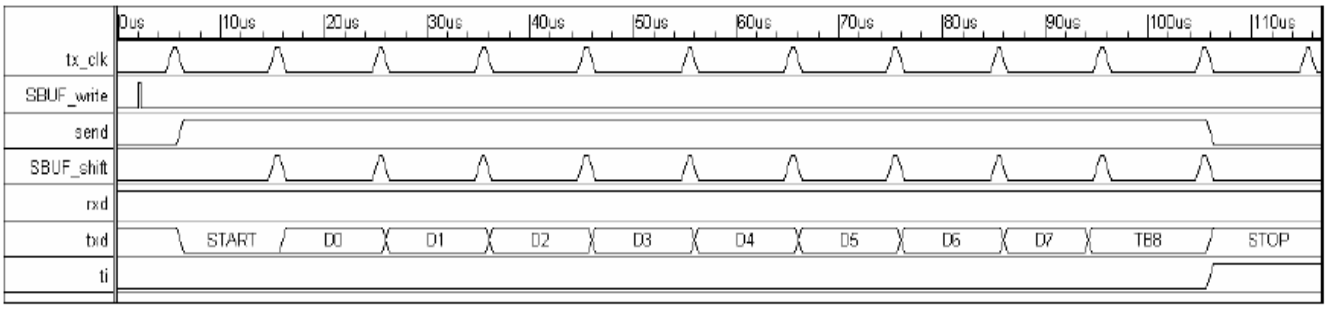


Figure 17-4: UARTn communication mode 3 timing diagram

18. SPI MODULE

18.1 SPI Introduction

The SPI is a fully configurable SPI master/slave device, which allows user to configure polarity and phase of serial clock signal SCK. The SPI allows the microcontroller to communicate with serial peripheral devices. It is also capable of inter process or communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received. The SPI is a technology independent design that can be implemented in a variety of process technologies.

The SPI system is flexible enough to interface directly with many standard product peripherals from multiple manufacturers. The system can be configured as either a master or a slave device. To accommodate most of the available synchronous serial peripherals, the clock control logic allows selection of clock polarity, and two different clock protocols. When the SPI is configured as a master device, the software selects one of eight different bit rates for the serial clock.

The SPI automatically drive selected by SSCR (Slave Select Control Register) slave select NSS outputs, and address SPI slave device to exchange serially shifted data. Error-detection logic is included to support inter process or communications. A write conflict detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detects or automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to become bus master.

The characteristics of SPI are as follows:

- Full duplex synchronous serial data transfer;
- Master mode and Slave mode supported;
- Multi-master system supported;
- System error detection;
- Interrupt generation;
- Supports speeds up to ¼ of system clock (F_{SYS}≤24MHz);
- Bit rates generated 1/4, 1/8, 1/ 16, 1/32, 1/64, 1/128, 1/256, 1/512 of system clock;
- Four transfer formats supported;
- Simple interface allows easy connection to microcontrollers.

18.2 SPI Port Configuration

To use the SPI function, you must first configure the SPI-related registers, and then configure the corresponding port as an SPI channel (any GPIO can be configured as an SPI channel), such as configuring P1.4 as an NSS channel, P1.5 as a SCLK channel, P1.6 as a MOSI channel, and P1.7 as a MISO channel, with the following configuration code:

```
P14CFG = 0x0E;  // P1.4 is configured as a NSS channel
P15CFG = 0x0F;  // P1.5 is configured as a SCLK channel
P16CFG = 0x10;  // P1.6 is configured as a MOSI channel
P17CFG = 0x11;  // P1.7 is configured as a MISO channel
```

The ports are configured as SCLK, MOSI, MISO and NSS, with pull-up resistors and open-drain output switches forced off. The schematic diagram of the multi-machine SPI communication structure is shown below.

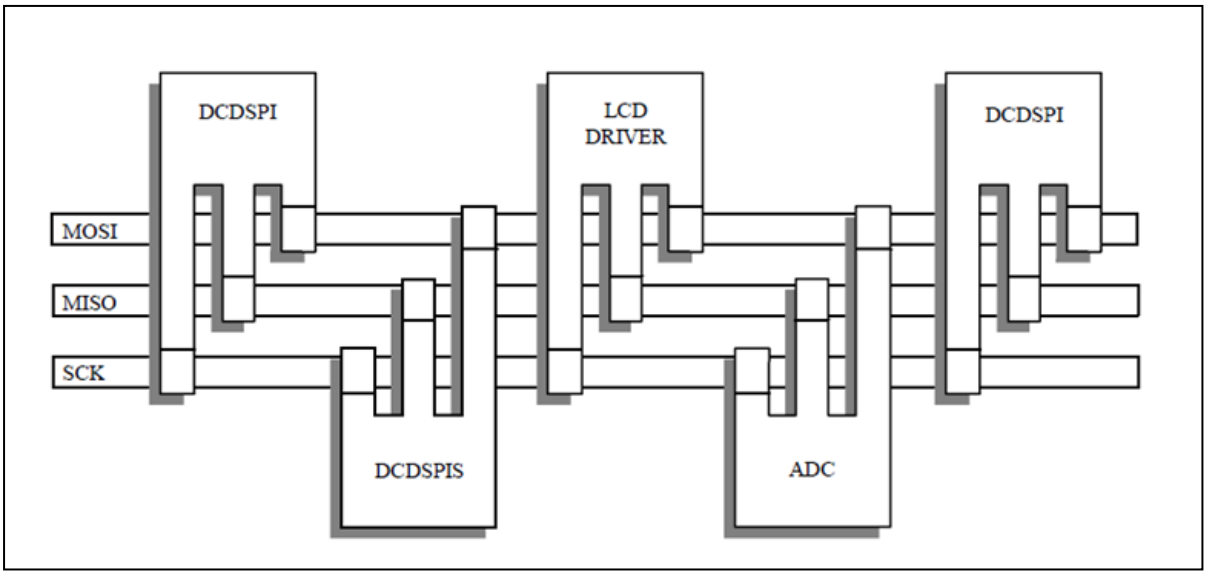


Figure 18-1: Multiple SPI communication

18.3 SPI Block Diagram

When an SPI transfer occurs, an 8-bit character is shifted out on data pin while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.

The central element in the SPI system is the block containing the shift register and the read data buffer. The system is single buffered in the transmit direction and double buffered in the receive direction. This fact means new data for transmission cannot be written to the shifter until the previous transaction is complete; however, received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial character. As long as the first character is read out of the read data buffer before the next serial character is ready to be transferred, no overrun condition will occur.

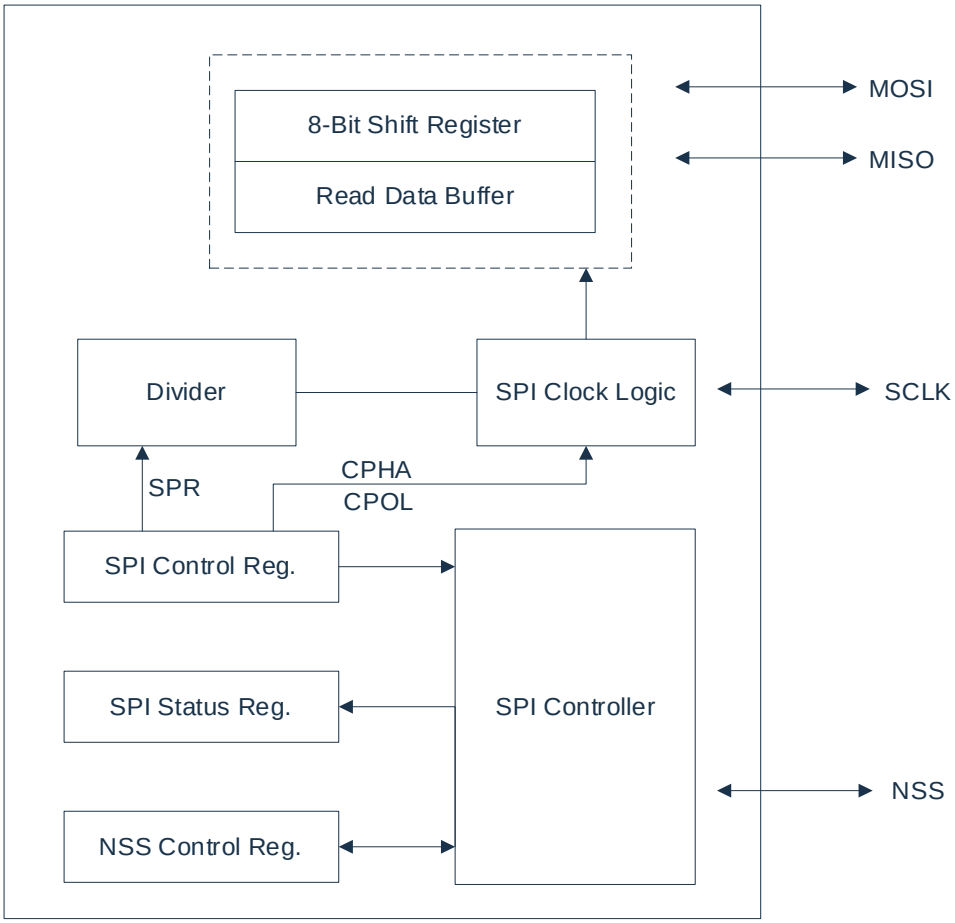


Figure 18-2: SPI block diagram

The eight pins are associated with the SPI: NSS, SCLK, MOSI, MISO.

The NSS input pin in master mode is used to detect mode errors. A low level on this pin indicates that another device in the multi-master system has become the master device and is attempting to select the SPI as the slave device. The NSS input pin in slave mode is used to enable transmission.

In master mode, the SCLK pin is used as the SPI clock signal reference. When the master device initiates a transmission, eight clock cycles are automatically generated on the SCLK pin.

- When the SPI is configured as a slave, the SI pin is the slave input data line, and the SO is the slave output data line.
- When the SPI is configured as a master, the MI pin is the master input data line, and the MO is the master output data line.

18.4 SPI Related Registers

18.4.1 SPI Control Register (SPCR)

0xEC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPCR	--	SPEN	SPR2	MSTR	CPOL	CPHA	SPR1	SPR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	1	0	0

Bit7 --

Bit6 SPEN: SPI mode enable

1= Enable;

0= Disable.

Bit5 SPR2: SPI clock rate select :[2].

Bit4 MSTR: SPI mode select;

1= master mode;

0= slave mode.

Bit3 CPOL: SPI clock polarity select;

1= SCLK is high in idle state;

0= SCLK is low in idle state.

Bit2 CPHA: SPI clock phase select.

Bit1~Bit0 SPR1-SPR0: SPI clock rate select :[1:0]

(See the table below for frequency control details)

SPR2-SPR0 control SPI clock divider

SPR2	SPR1	SPR0	System clock divided by
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64
1	0	1	128
1	1	0	256
1	1	1	512

Note: The SPI clock supports up to 8 divisions of the system clock at 48MHz, i.e. 6MHz.

18.4.2 SPI Data Register (SPDR)

0xEE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPDR	SPIDATA7	SPIDATA6	SPIDATA5	SPIDATA4	SPIDATA3	SPIDATA2	SPIDATA1	SPIDATA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 SPIDATA<7:0>: Data sent or received by the SPI.
Write: Write the data to be sent (Send order from MSB to LSB).
Read: Received data.

18.4.3 SPI Slave Select Control Register (SSCR)

The control register may be read or written at any time. It is used to configure which slave select output should be driven while SPI master transfer. Contents of SSCR register is automatically assigned on NSS pins when SPI master transmission starts.

0xEF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SSCR	--	--	--	--	--	--	--	SSO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit7~Bit1 -- Reserved, and it must be 1.
Bit0 SSO0: SPI slave device selection control bit.
0= When SPI host transmission starts, NSS output 0.
1= When SPI host transmission starts, NSS output 1.

18.4.4 SPI State Register (SPSR)

0xED	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPSR	SPISIF	WCOL	--	--	--	--	--	SSCEN
R/W	R	R	--	R	--	--	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPISIF: SPI complete flag, Read only;
1= SPI transfer to complete (Read SPSR first, then clear after reading/writing SPDR);
0= SPI not transferred.
Bit6 WCOL: SPI write conflict error flag Read only;
1= SPI write conflict error (Read SPSR first, then clear after reading/writing SPDR);
0= No write conflict error.
Bit5~ Bit2 --
Bit1 Reserved: It must be 0
Bit0 SSCEN: SPI master control mode NSS output control bit.
1= NSS outputs high when SPI is being in idle state;
0= NSS outputs the content of register SSCR.

SPI status register (SPSR) contains flags indicating the completion of transfer or occurrence of system errors. All flags are set automatically when the corresponding event occur and cleared by software sequence. SPIF and WCOL are automatically cleared by reading SPSR followed by an access of the SPDR.

The SSCEN bit is the enable bit for the automatic slave selection output. When SSCEN is set to 1, the NSS line outputs the contents of the SSCR register when the transmission is in progress, and the NSS goes high when the transmission is idle. When the SSCEN bit is cleared to zero, the NSS line always displays the contents of the SSCR register.

18.5 SPI Master Mode

When the SPI is configured in master mode, the transfer is initiated by writing to the SPDR register. When a new byte is written to the SPDR register, the SPI starts the transfer. The serial clock, SCLK, is generated by the SPI and is enabled by the SPI in master mode and output by SCLK.

The SPI in master mode can select SPI slave devices via the NSS line. The NSS line-slave select output line loads the contents of register SSCR[0]. The SSCEN bit of the SPSR register selects between automatic NSS line control and software control. With the SSCEN bit in master mode, when SSCEN is set to 1, the NSS line outputs the contents of the SSCR register while the transmission is in progress, and the NSS goes high when the transmission is idle. When the SSCEN bit is cleared, the NSS line is controlled by software and always displays the contents of the SSCR register, regardless of whether the transmission is in progress or the SPI is idle.

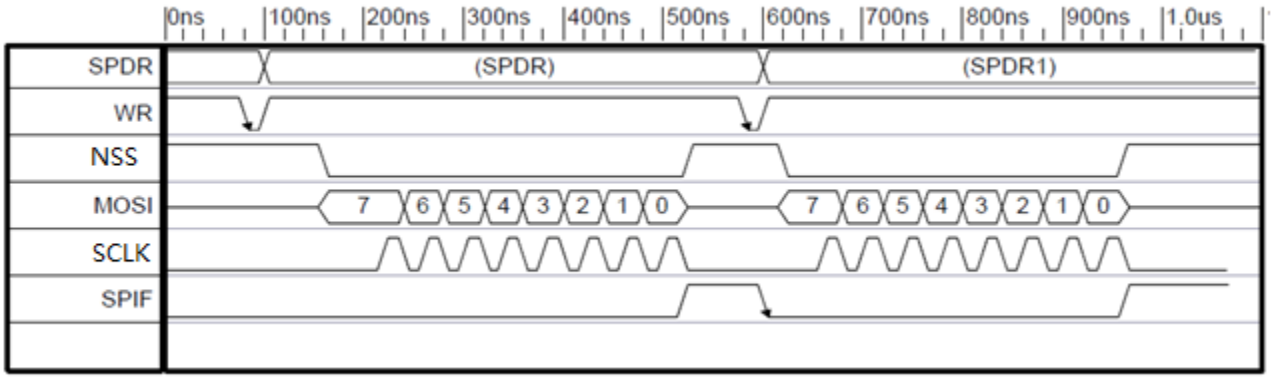


Figure 18-3: Automatic slave selection line usage

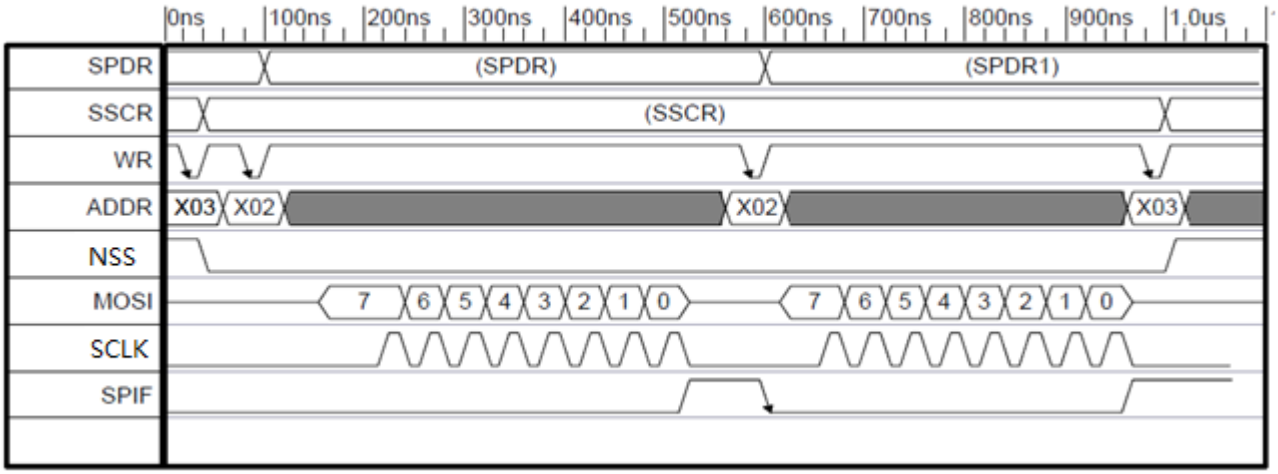


Figure 18-4: Software controlled NSSx line

18.5.1 Write Conflict Error

A write conflict occurs if the SPI data register is written while a transfer is in progress. The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. The write conflict is indicated by the WCOL flag in SPSR (3) register.

The WCOL flag is set automatically by hardware when the WCOL error condition occurs. To clear the WCOL bit, user should execute the following steps:

- Read contents of the SPSR register
- Access to the SPDR register (read or write)

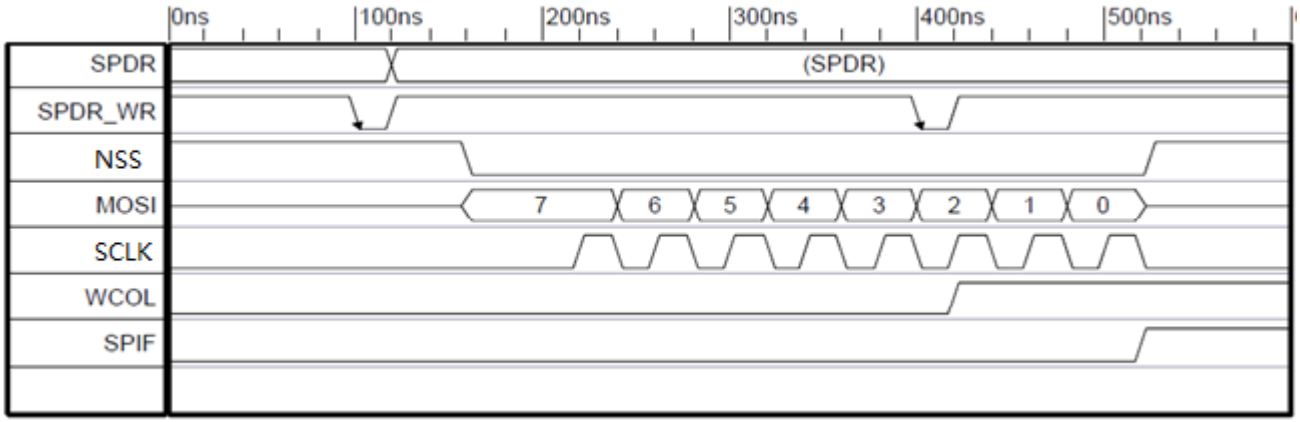


Figure 18-5: Write conflict error in SPI master mode

The conditions for writing conflicts: During data transmission, when NSS is low, the first data starts transmitting to the 8th SCLK falling edge. If SPDR is written during this time, a write conflict will occur and WCOL will be set.

Warning: When starting to send data, if NSS does not immediately go low after writing SPDR, needs to wait for up to one SPI clock before it starts low. After NSS is low, it needs to wait for a system clock to start sending the first data, and then enter the real data transmission state. Writing to SPDR again does not create a write conflict while writing SPDR to enter the true data transfer state. However, this operation updates the data to be sent. If there are multiple writes to SPDR, the data sent will be the last value written to SPDR.

Since the SPI has only one transmit buffer, it is recommended to judge whether the last data has been sent before writing the SPDR, and then confirm that the SPDR register is written after the transmission is completed to prevent a write conflict.

18.6 SPI Slave Mode

When configured as SPI Slave the DSPI transfer is initiated by external SPI master module by assertion of the SPI Slave Select input, and generation of the SCK serial clock.

Before the transfer begins, it is necessary to determine which SPI slave will be used to exchange data. When NSS is used, the clock signal connected to the SCLK line will cause the SPI slave device to shift the contents of the receive shift register to the MOSI line and drive the MISO line with the contents of the transmitter shift register. When all 8 bits are shifted in/out, the SPI generates an interrupt request by setting the IRQ output. The contents of the shift register drive the MISO line.

In SPI slave mode, there can be only one transmission error (write conflict error).

18.6.1 Addressed Error

In slave mode, only write conflict errors can be detected by the SPI.

A write conflict error occurs when an SPDR register write operation is performed while an SPI transfer is in progress.

In slave mode, a write conflict error may occur when the CPHA is cleared, even if all bits have been transferred, as long as the NSS slave select line is driven low. This is because the start of the transfer is not explicitly specified, and the fact that the NSS is driven low after a full byte transfer may indicate the start of the next byte transfer.

18.6.2 Write Conflict Error

A write conflict occurs if the DSPI data register is written while a transfer is in progress. The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. The write conflict is indicated by the WCOL flag in SPSR (3) register.

The WCOL flag is set automatically by hardware, when the WCOL error condition occurs. To clear the WCLO bit, user should execute the following sequence:

- read contents of the SPSR register;
- access to the SPDR register (read or write).

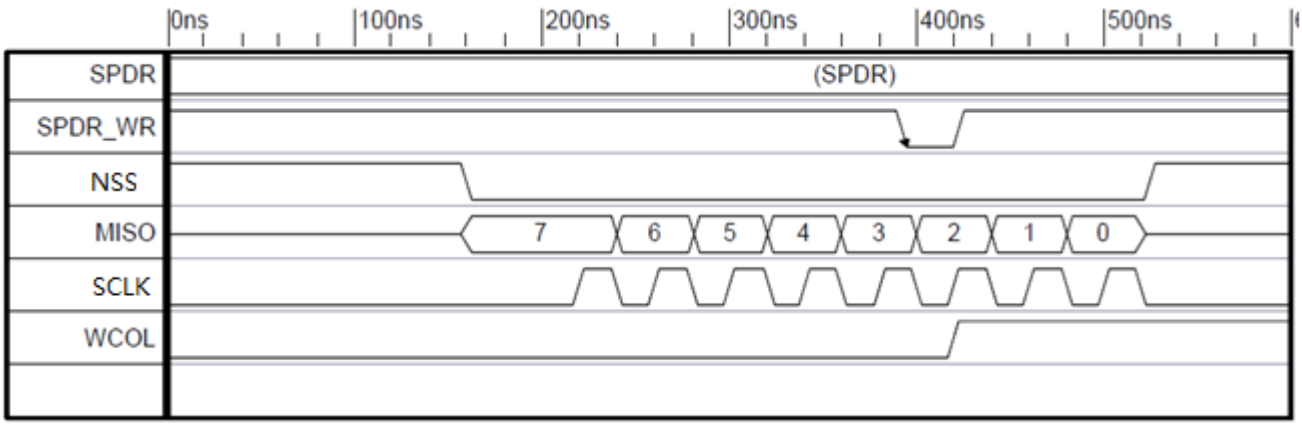


Figure 18-6: Write Conflict Error - SPI Slave mode – SPDR write during transfer

Figure below shows the WCOL generation, in case that the CPHA is cleared. As it is shown the WCOL generation is cause by any S{DR register write with NSS line cleared. It is done even if the SPI master didn’t

generate the serial clock SCK. This is because there is not clearly specified the transfer beginning, and NSS driven low after full byte transfer may indicate beginning of the next byte transfer.

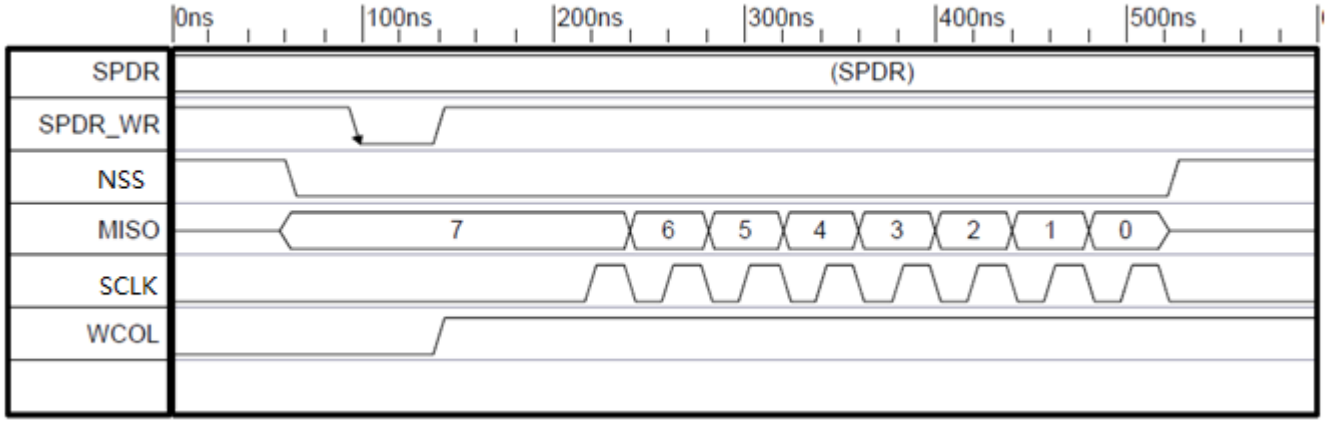


Figure18-7: WCOL Error-SPI Slave mode–SPDR write when CPHA = 0 and NSS = 0

After the SPDR is written in the slave mode, the host-controlled NSS does not go low immediately. When NSS is low, it needs to wait for the second edge of SCLK to start to enter the real data transmission state.

Writing to SPDR does not create a write conflict during the SPDR to start sending the first data. However, this operation updates the data to be sent. If there are multiple writes to SPDR, the data sent will be the last value written to SPDR.

During the start of the first data transmission to the second edge of SCLK, writing to SPDR again does not create a write conflict and does not update the data being transmitted. That is, the operation of writing the SPDR is ignored.

Since the SPI has only one transmit buffer, it is recommended to judge whether the last data is sent before writing SPDR, and then confirm that the SPDR register is written after the transmission is completed to prevent write conflict.

18.7 SPI Clock Control Logic

18.7.1 SPI Clock Phase and Polarity Control

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the SPI allows direct interface to almost any existing synchronous serial peripheral.

18.7.2 SPI Transmit Format

During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device; slave devices that are not selected do not interfere with SPI bus activities. On a master SPI device, the slave select line can optionally be used to indicate a multiple-master bus contention.

18.7.3 CPHA=0 Transmit Format

Figure below shows a timing diagram of an SPI transfer where CPHA is 0. Two waveforms are shown for SCK: one for CPOL equals 0 and another for CPOL equals 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, master in/slave out (MISO), and master out/slave in (MOSI) pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The NSS line is the slave select input to the slave; the NSS pin of the master is not shown but is assumed to be inactive. The NSS pin of the master must be high. This timing diagram functionally depicts how a transfer takes place; it should not be used as a replacement for data-sheet parametric information.

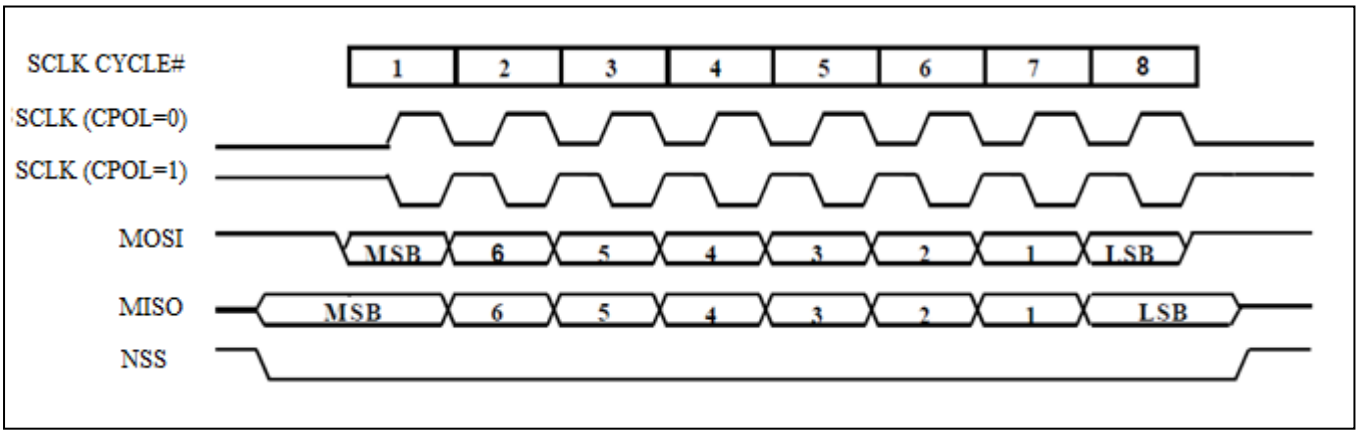


Figure 18-8: CPHA=0 SPI transmit format

When CPHA = 0, the NSS line must be deasserted and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while SS is active low, a write-conflict error results. When CPHA = 1, the NSS line may remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave driving the MISO data line.

18.7.4 CPHA=1 Transmit Format

Figure below is a timing diagram of an SPI transfer where CPHA = 1. Two waveforms are shown for SCK: one for CPOL= 0 and another for CPOL = 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, MISO, and MOSI pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The SS line is the slave select input to the slave; the SS pin of the master is not shown but is assumed to be inactive. The SS pin of the master must be high or must be reconfigured as a general-purpose output not affecting the SPI.

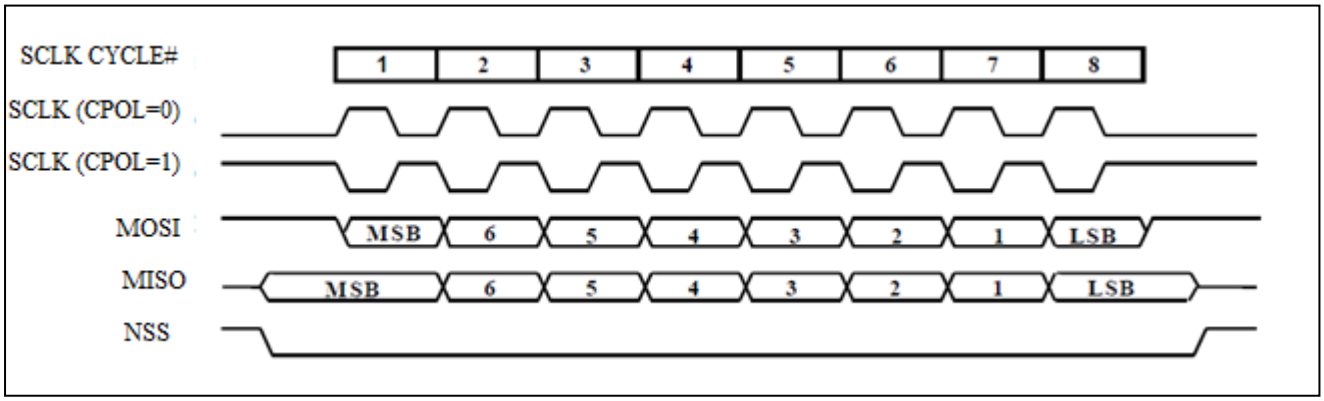


Figure 18-9: CPHA=1 SPI transmit format

18.8 SPI Data Transmission

18.8.1 SPI Transmission Start

All SPI transfers are started and controlled by a master SPI device. As a slave, the DSPI considers a transfer to begin with the first SCK edge or the falling edge of NSS, depending on the CPHA format selected. When CPHA = 0, the falling edge of SS indicates the beginning of a transfer. When CPHA = 1, the first edge on the SCK indicates the start of the transfer. In either CPHA format, a transfer can be aborted by taking the SS line high, which causes the SPI slave logic and bit counters to be reset. The SCK rate selected has no effect on slave operations since the clock from the master is controlling transfers.

When the SPI is configured as a master, transfers are started by a software write to the SPDR.

18.8.2 SPI Transmission End

An SPI transfer is technically complete when the SPIF flag is set, but, depending on the configuration of the SPI system, there may be additional tasks. Because the SPI bit rate does not affect timing of the ending period, only the fastest rate is considered in discussions of the ending period. When the SPI is configured as a master, SPIF is set at the end of the eighth SCK cycle. When CPHA equals 1, SCK is inactive for the last half of the eighth SCK cycle.

When the SPI is operating as a slave, the ending period is different because the SCK line can be asynchronous to the MCU clocks of the slave and because the slave does not have access to as much information about SCK cycles as the master. For example, when CPHA = 1, where the last SCK edge occurs in the middle of the eighth SCK cycle, the slave has no way of knowing when the end of the last SCK cycle is. For these reasons, the slave considers the transfer complete after the last bit of serial data has been sampled, which corresponds to the middle of the eighth SCK cycle.

The SPIF flag is set at the end of a transfer, but the slave is not permitted to write new data to the SPDR while the NSS line is still low.

18.9 SPI Timing Diagram

18.9.1 Master Mode Transmission

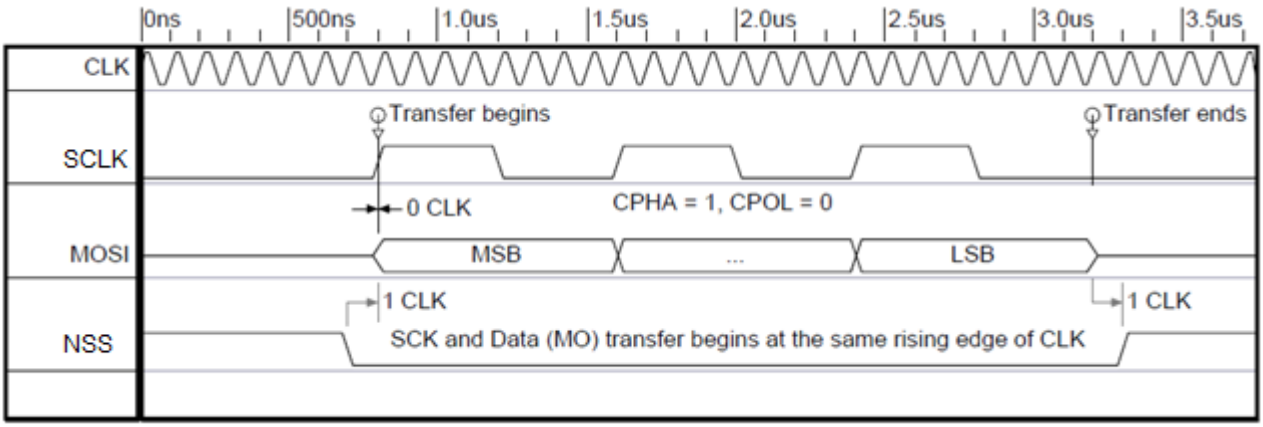


Figure 18-10: Master mode timing diagram

18.9.2 Slave Mode Transmission

At a beginning of transfer in Slave mode the data on serial output (MISO) appears on first rising edge after falling edge on Slave Select (NSS) line.

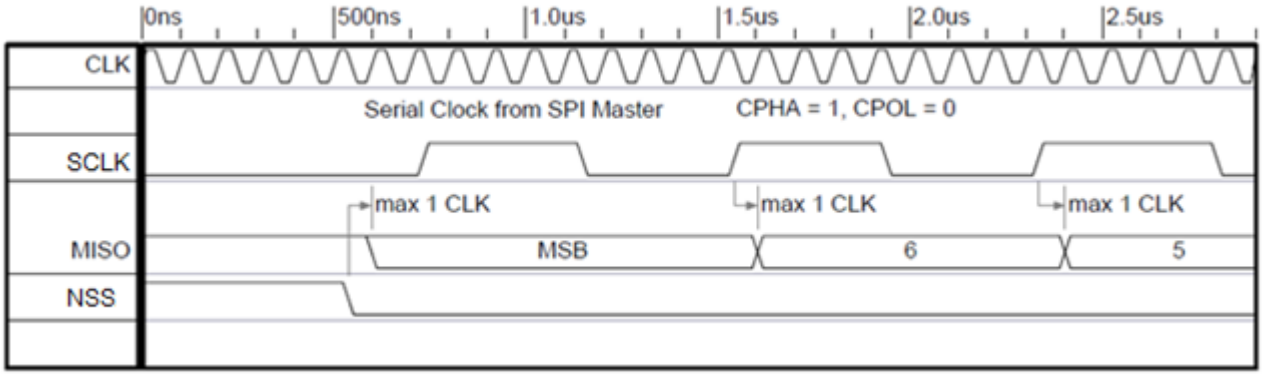


Figure 18-11: Slave mode timing diagram

18.10 SPI Interrupt

SPI's interrupt number is 22,The interrupt vector is 0x00B3. If the SPI interrupt is to be enabled, the SPIIE must be set to 1, and set the total interrupt EA.

If the SPI related interrupt enable is turned on and the SPI total interrupt indication bit SPIIF = 1, the CPU will enter the interrupt service routine. SPIIF operation attributes are read-only and independent of the state of SPIIE.

After the SPI status register SPSR has the transfer completion flag SPISIF, write conflict WCOL, and mode error MODF, the SPI total interrupt indication bit, SPIIF, will be set. SPIIF is automatically cleared only when all three flags are 0.

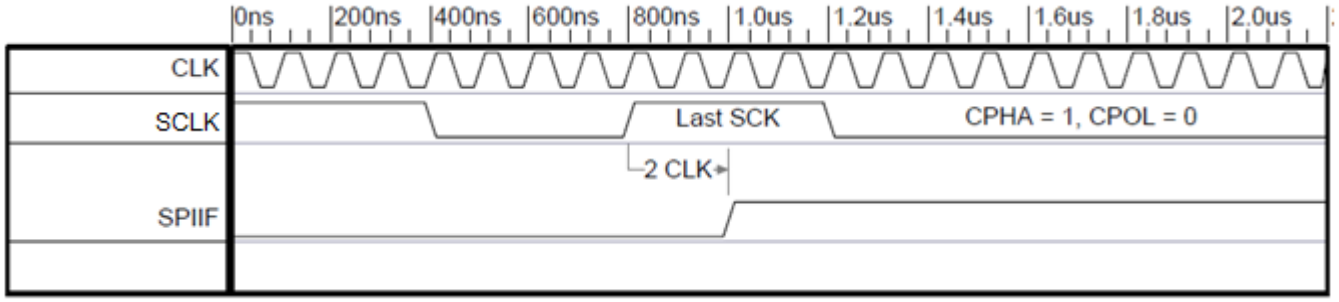


Figure 18-12: Interrupt generation

Interrupt Mask Register (EIE2)

0xAA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIE2	SPIIE	I2CIE	WDTIE	ADCIE	PWMIE	--	ET4	ET3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPIIE: SPI Interrupt enable bit
1= Enable SPI interrupt;
0= Disable SPI interrupt.

Bit6 I2CIE: I^2C Interrupt enable bit
1= Enable I^2C interrupt;
0= Disable I^2C interrupt.

Bit5 WDTIE: WDT Interrupt enable bit
1= Enable WDT interrupt;
0= Disable WDT interrupt.

Bit4 ADCIE ADC Interrupt enable bit
1= Enable ADC interrupt;
0= Disable ADC interrupt.

Bit3 PWMIE: PWM global interrupt enable bit
1= Enable PWM global interrupt;
0= Disable PWM global interrupt.

Bit2 --

Bit1 ET4: Time4 Interrupt enable bit
1= Enable Time4 interrupt;
0= Disable Time4 interrupt.

Bit0 ET3: Time3 Interrupt enable bit
1= Enable Time3 interrupt;
0= Disable Time3 interrupt.

Interrupt Priority Control Register (EIP2)

0xB8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIP2	PSPI	PI2C	PWDT	PADC	PPWM	--	PT4	PT3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 PSPI: SPI interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit6 PI2C: I^2C interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit5 PWDT: WDT interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit4 PADC: ADC interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit3 PPWM: PWM interrupt priority control bit
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit2 --

Bit1 PT4: TIMER4 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Bit0 PT3: TIMER3 interrupt priority control bit;
1= Set to advanced interrupt;
0= Set to low level interrupt.

Peripheral Interrupt Flag Register (EIF2)(0xB2)

0xB2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIF2	SPIIF	I2CIF	--	ADCIF	PWMIF	--	TF4	TF3
R/W	R	R	--	R/W	R	--	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 SPIIF: SPI total interrupt indicator bit, read-only;
1= SPI generated interrupt, (this bit is automatically cleared when the specific interrupt flag bit is cleared);
0= SPI does not generate interrupts.
Bit6 I2CIF: I^2C total interrupt indication bit, read-only;
1= I^2C generates an interrupt, (this bit is automatically cleared when the specific interrupt flag bit is cleared);
0= I^2C does not generate an interrupt.
Bit5 --
Bit4 ADCIF: ADC interrupt flag bit;
1= Completion of ADC conversion, requiring software clearing;
0= ADC conversion is not completed.
Bit3 PWMIF: PWM total interrupt indicator bit, read-only;
1= PWM generates an interrupt, (this bit is automatically cleared when the specific interrupt flag bit is cleared);
0= PWM does not generate interrupts.
Bit2 --
Bit1 TF4: Timer4 counter overflow interrupt flag bit;
1= Timer4 counter overflow, which is automatically cleared by hardware when entering the interrupt service routine, or can be cleared by software;
0= Timer4 counter without overflow.
Bit0 TF3: Timer3 counter overflow interrupt flag bit;
1= Timer3 counter overflow, which is automatically cleared by hardware when entering the interrupt service program, or by software;
0= Timer3 counter without overflow.

19. ACMP MODULE

The chip contains two internal analog comparators. The comparators can be configured to suit different applications. When the positive terminal voltage is greater than the negative terminal voltage, the comparator outputs logic 1, otherwise it outputs 0, which can also be changed by the output polarity selection bit. When the output value of the comparator changes, each comparator can generate an interrupt.

19.1 Comparator Characteristics

The comparator has the following characteristics:

- Analog input voltage range: 0~(VDD-1.5)V
- Selectable 5 port inputs and 1 PGA output per comparator positive terminal
- The negative terminal of each comparator can select the port input CnN and the internal reference voltage VREF
- The internal reference voltage can choose the internal Bandgap (1.2V) and ACMP_VREF output.
- ACMP_VREF reference source voltage divider range: k=(2/20)~(17/20), a total of 16 gear selections.
- The output filter time can be selected: 0~512*Tsys.
- Support unilateral (positive/negative) and bilateral (positive and negative) hysteresis control.
- The hysteresis voltage can be 10/20/60mV.
- The software supports offset voltage trimming.
- The output can be used as an enhanced PWM brake trigger signal.
- An output change can generate an interrupt.

19.2 Comparators Structure

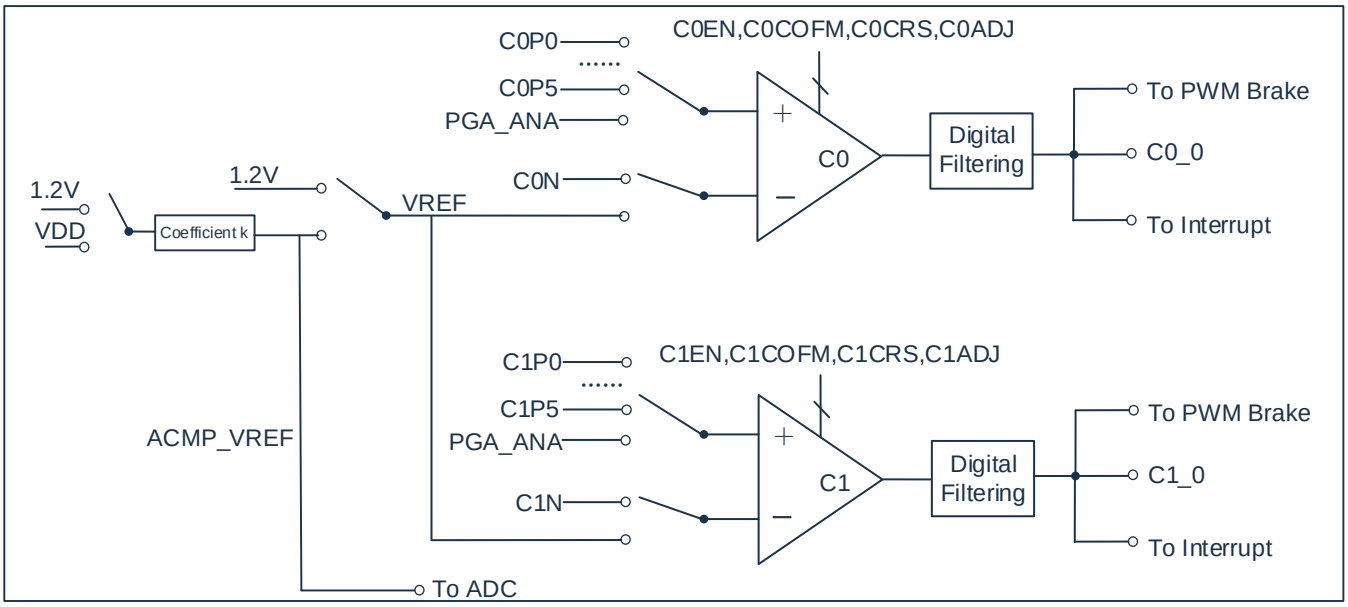


Figure 19-1: Comparator structure diagram

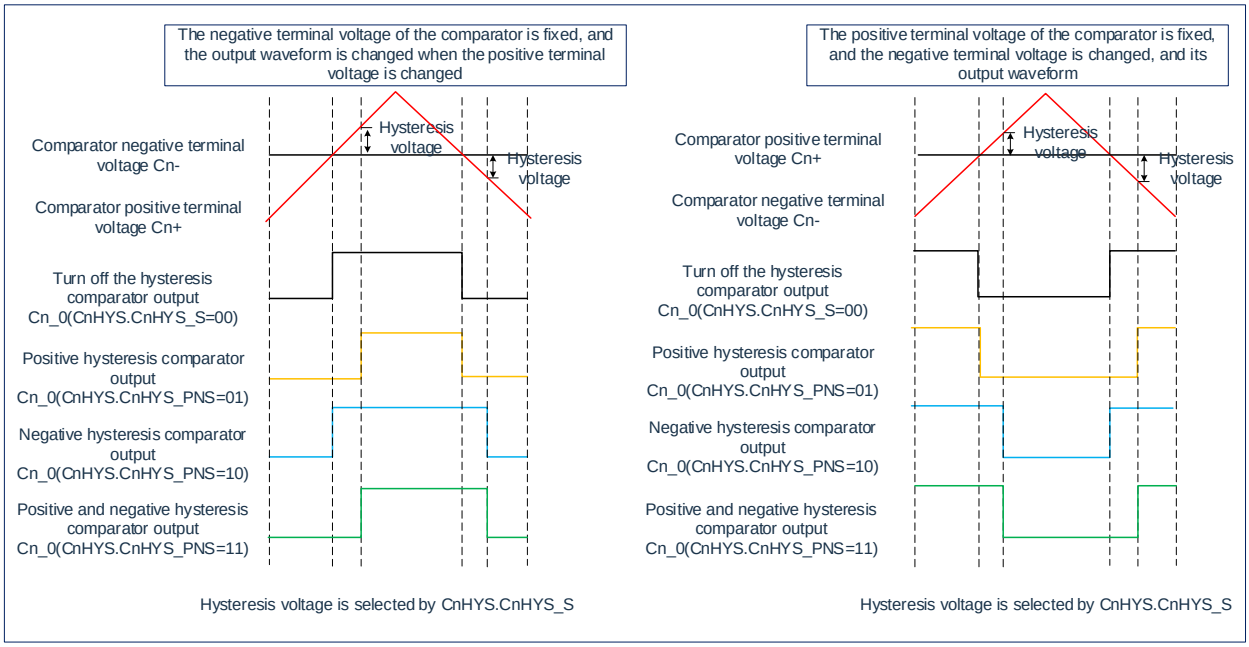


Figure 19-2: Hysteresis control structure block diagram

19.3 Comparator Related Registers (n=0,1)

CnCON0 Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CnCON0	CnEN	CnCOFM	CnN2G	CnNS1	CnNS0	CnPS2	CnPS1	CnPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

C0CON0 address: F500H; C1CON0 address: F503H.

Bit7 CnEN: Comparator n enable bit;
1= Enable;
0= Disable.

Bit6 CnCOFM: Comparator n adjustment mode enable bit;
1= Enable adjustment mode;
0= Disable adjustment mode.

Bit5 CnN2G: Comparator n adjustment mode negative terminal grounding enable bit (this bit is valid when CnCRS=0);
1= Negative terminal channel is closed and the internal negative terminal is grounded;
0= Negative terminal channel is enabled, and the signal is input from the negative terminal.

Bit4~Bit3 CnNS<1:0>: Comparator n negative channel selection bit;
00= CnN;
01= Internal voltage (Bandgap or ACMP_VREF);
1x= Reserved, prohibited to use.

Bit2~Bit0 CnPS<2:0>: Comparator n positive channel selection bit CnPS<2:0>;
000= CnP0;
001= CnP1;
010= CnP2;
011= Reserved, prohibited to use;
100= CnP4;
101= CnP5;
110= PGA_ANA;
111= Reserved, prohibited to use.

CnCON1 Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CnCON1	CnOUT	CnCRS	--	CnADJ4	CnADJ3	CnADJ2	CnADJ1	CnADJ0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1	0	0	0	0

C0CON1 address: F501H; C1CON1 address: F504H.

Bit7 CnOUT: Comparator n result bit (read-only);

Bit6 CnCRS: Comparator n adjustment mode input terminal selection;
1= Connect the positive and negative terminals together and input from the positive terminal;
0= Connect the positive and negative terminals together, from the negative terminal enter.

Bit5 Reserved

Bit4~ Bit0 CnADJ<4:0>: Comparator n offset voltage adjustment bits.

CnCON2 Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CnCON2	--	--	CnPOS	CnFE	CnFS3	CnFS2	CnFS1	CnFS0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

C0CON2 address: 0xF502; C1CON2 address: 0xF505.

Bit7~Bit6 --

Bit5 CnPOS: Comparator n output polarity selection bit (can cause interrupt flag bit position when switching);
1= Inverted output;
0= Normal output .

Bit4 CnFE: Comparator n output filter enable bit;
1= Enable filtering;
0= Disable filtering.

Bit3~Bit0 CnFS<3:0>: Comparator n output filter time selection bit.
0000= (0~1)*Tsys
0001= (1~2)Tsys
0010= (2~3)Tsys
0011= (4~5)Tsys
0100= (8~9)Tsys
0101= (16~17)Tsys
0110= (32~33)Tsys
0111= (64~65)Tsys
1000= (128~129)Tsys
1001= (256~257)Tsys
1010= (512~513)Tsys
Other= (0~1)*Tsys

CNVRCON Register

F506H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CNVRCON	--	--	CNDIVS	CNSVR	CNVS3	CNVS2	CNVS1	CNVS0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit5 -- Reserved, must all be 0.

Bit5 CNDIVS: ACMP_VREF reference source selection bit;
1= Select 1.2V (Bandgap) for voltage division;
0= Select VDD for voltage division.

Bit4 CNSVR: Comparator negative terminal internal voltage VREF selection bit;
1= Select ACMP_VREF (the voltage divider circuit is turned on, independent of the comparator module);
0= Select 1.2V (Bandgap).

Bit3~Bit0 CNVS<3:0>: ACMP_VREF reference source voltage divider coefficient k selection bits;
0000-1111= 2/20 ~ 17/20.

CNFBCON Register

F507H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CNFBCON	--	--	--	--	C1FBEN	C0FBEN	C1FBLS	C0FBLS
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit4 --

Bit3 C1FBEN: Comparator 1 output control PWM brake enable bit;
0= disable;
1= enable.

Bit2 C0FBEN: Comparator 0 output control PWM brake enable bit;
0= disable;
1= enable.

Bit1 C1FBLS: Comparator 1 output control PWM brake edge selection bit;
0= rising edge;
1= falling edge.

Bit0 C0FBLS: Comparator 0 output control PWM brake edge selection bit;
0= rising edge;
1= falling edge.

CNIE Register

F508H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CNIE	--	--	--	--	--	--	C1IE	C0IE
R/W	R	R	R	R	R	R	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit2 --

Bit1 C1IE: Comparator 1 interrupt enable bit;
0= disable;
1= enable.

Bit0 C0IE: Comparator 0 interrupt enable bit;
0= disable;
1= enable.

CNIF Register

F509H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CNIF	--	--	--	--	--	--	C1IF	C0IF
R/W	R	R	R	R	R	R	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~ Bit2 --

Bit1 C1IF: Comparator 1 interrupt flag bit (write 0 to clear);
1= Comparison 1 output has changed.
0= -

Bit0 C0IF: Comparator 0 interrupt flag bit (write 0 to clear);
1= Compare 0 output has changed.
0= -

CnADJE Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CnADJE	CnADJE7	CnADJE6	CnADJE5	CnADJE4	CnADJE3	CnADJE2	CnADJE1	CnADJE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

C0ADJE address: F50AH; C1ADJE address: F50BH.

Bit7~Bit0 CnADJE<7:0>: Comparator n offset voltage adjustment mode selection;
AAH = determined by CnADJ<4:0> in CnCON1 register;
Others= determined by CONFIG related bits.

It is recommended to start the comparator after setting the parameters of the comparator, otherwise, the output jump of the comparator may be detected by mistake during the setting process.

CnHYS Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CnHYS	--	--	--	--	CnHYS_PNS1	CnHYS_PNS0	CnHYS_S1	CnHYS_S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

C0HYS address: F50CH; C1HYS address: F50DH.

Bit7~Bit4 --

Bit3~Bit2 CnHYS_PNS<1:0> positive and negative hysteresis selection bits;
00= turn off hysteresis;
01= positive hysteresis (unilateral hysteresis);
10= negative hysteresis (unilateral hysteresis);
11= positive and negative hysteresis (bilateral hysteresis).

Bit1~ Bit0 CnHYS_S<1:0> hysteresis control bit;
00= turn off hysteresis;
01= 10mV
10= 20mV
11= 60mV

20. OP MODULE

The chip contains two op-amp modules. A small number of peripheral components can be used to achieve the basic signal amplification and signal calculation functions.

20.1 Op-Amp Characteristics

Operational amplifier has the following characteristics:

- Three terminals of each op amp are multiplexed with GPIO port.
- The positive terminal supports internal 1.2V voltage input.
- Supports comparison of two modes.
- Op-amp output can be connected to internal analog comparator input for shaping.
- The output of the op amp can be connected to the 31 channels inside the ADC for measurement.
- The software supports offset voltage trimming.

20.2 Op-Amp Structure

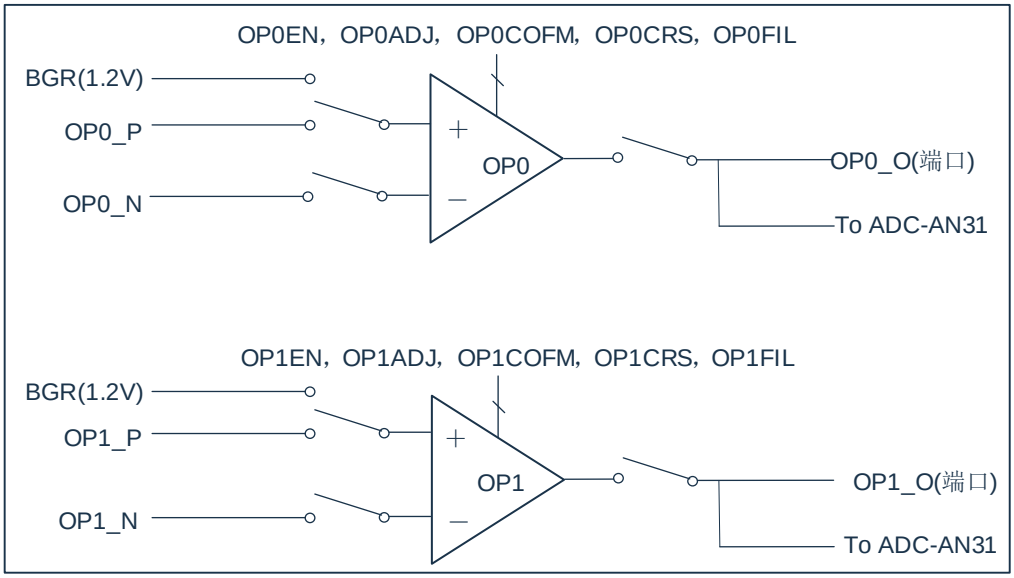


Figure 20-1: Op-amp structure diagram

20.3 20.3 Op-Amp Related Registers

OPnCON0 Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPnCON0	OPnEN	OPnCOFM	OPnFIL	OPnOS	OPnNS1	OPnNS0	OPnPS1	OPnPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	0	0	0	0	0

OP0CON0 address: F520H; OP1CON0 address: F523H.

Bit7 OPnEN: OPn enable bit;
1= Enable;
0= Disable.

Bit6 OPnCOFM: OPn adjustment mode enable bit;
1= Enable;
0= Disable.

Bit5 OPnFIL: OPn working mode selection;
1= Operation amplifier mode (OPnCOFM must be 0);
0= Comparison mode (OPnCOFM must be 0).

Bit4 OPnOS: OPn output channel selection bit;
1= OPn_O;
0= Disable.

Bit3~Bit2 OPnNS<3:2>: OPn negative terminal channel selection bits;
00= OPn_N;
others = Prohibited.

Bit1~Bit0 OPnPS<1:0>: OPn positive channel selection bits;
00= OPn_P;
01= BGR (1.2V);
others = Prohibited.

OPnCON1 Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPnCON1	OPnDOUT	OPnCRS	--	OPnADJ4	OPnADJ3	OPnADJ2	OPnADJ1	OPnADJ0
R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1	0	0	0	0

OP0CON1 address: F521H; OP1CON1 address: F524H.

Bit7 OPnDOUT: OPn adjustment result bit/comparison mode output, read only.

Bit6 OPnCRS: OPn adjustment mode input terminal selection;
1= Positive terminal input (only OPn_P can be selected);
0= Negative terminal input.

Bit5 --

Bit4~Bit0 OPnADJ<4:0>: OPn offset voltage adjustment bits.

OPnADJE Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPnADJE	OPnADJE7	OPnADJE6	OPnADJE5	OPnADJE4	OPnADJE3	OPnADJE2	OPnADJE1	OPnADJE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

OP0ADJE address: F526H; OP1ADJE address: F527H.

Bit7~Bit0 OPnADJE<7:0>: OPn offset voltage adjustment mode selection;

AAH = Determined by OPnADJ<4:0> in OPnCON1 register;

others= Determined by CONFIG related bits.

21. PGA MODULE

The chip contains a programmable gain amplifier module, and basic signal amplification functions can be implemented inside the chip.

21.1 PGA Characteristics

Its characteristics are as follows:

- Support PGA output test
- PGA input with sample-and-hold circuit
- PGA output can be connected to internal analog comparator input for shaping
- PGA output can be internally connected to ADC channel 31 for measurement
- Software support for offset voltage trimming
- Multi-level gain selectable (1/2/4/8/16/32/64/128)
- Supports single-ended/pseudo-differential inputs

The PGA supports normal amplification mode and sample hold mode, and the default is sample hold mode.

If the PGA input sample hold mode is not selected (PGANSHEN=1), the PGA input is amplified and the PGA_ANA is output. When PGA_ANA is converted to output by ADC, the ADC starts conversion immediately after the ADC conversion start bit is set to 1 until the conversion is finished.

If the PGA input sample hold mode (PGANSHEN=0) is selected, the PGA must be used in conjunction with an ADC for the PGA to output properly. When the PGA is in sample hold mode, the ADC channel 31 input source is required to select PGA_ANA. When the ADC conversion start bit ADGO is set to 1, it will wait for the set sample hold time. The input signal of PGA is amplified and output to PGA_ANA, and then the ADC really starts to convert until the conversion is finished. The ADC sample hold time is selected by register PGACON1[3:0].

21.2 PGA Structure

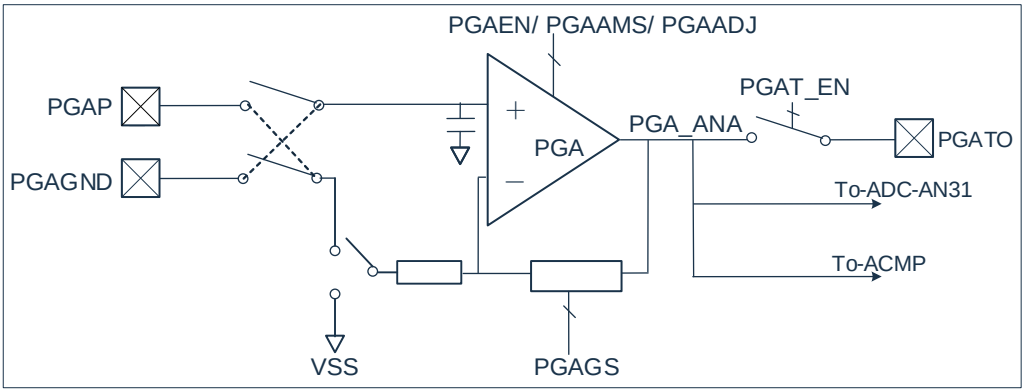


Figure 21-1: Block diagram of PGA structure

21.3 PGA Related Registers

PGACON0 Register

F529H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PGACON0	PGAEN	PGAGS2	PGAGS1	PGAGS0	PGAIMS1	PGAIMS0	PGAIPS1	PGAIPS0
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 PGAEN: The PGA enable bit;
1= Enable;
0= Disable.

Bit6~Bit4 PGAGS: PGA magnification selection;
000= 1 time;
001= 2 times;
010= 4 times;
011= 8 times;
100= 16 times;
101= 32 times;
110= 64 times;
111= 128 times.

Bit3~Bit2 PGAIMS<1:0>: PGA input mode selection bit.
00= Single-ended inputs.
others= Differential input (pseudo-differential)

Bit1~Bit0 PGAIPS<1:0>: PGA input port selection
00= Differential inputs: PGAP for the low-end input port and PGAGND for the high-end input port.
Single-ended input: Input port is PGAGND
others= Differential inputs: PGAP for the high input port and PGAGND for the low input port.
Single-ended input: Input port is PGAP

PGACON1 Register

F52AH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PGACON1	--	--	--	PGAAMS	PGASHT3	PGASHT2	PGASHT1	PGASHT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit5 --

Bit4 PGAAMS: PGA amplification mode selection bit.
1= Normal amplification mode
0= Sample hold mode
(Sample-and-hold circuit structure with ADC module. The sample hold is first performed at the PGA input and then amplified to the ADC conversion, which requires the cooperation of the PGA channel in ADC channel AN31 to be used).

Bit3~Bit0 PGASHT<3:0>: PGA sample hold time selection.
0000~1111= $1*T_{AD}$ ~$16*T_{AD}$.(T_{AD} is the sampling clock period of ADC).

PGACON2 Register

F52BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PGACON2	PGA_DOUT	--	--		PGAT_EN	--	--	
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7	PGA_DOUT	PGA regulation mode output (read-only bits).
	1=	Output 1.
	0=	Output 0.
Bit6~Bit4	--	Reserved.
Bit3	PGAT_EN	PGATO output enable control.
	1=	Enable.
	0=	Disable.
Bit2~Bit0	--	Reserved.

PGACON3 Register

F52CH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PGACON3	PGAMODE1	PGAMODE0	PGAADJ5	PGAADJ4	PGAADJ3	PGAADJ2	PGAADJ1	PGAADJ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	0	0	0	0	0

Bit7~Bit6	PGAMODE<1:0>:	PGA operating mode selection.
	00=	PGA normal mode.
	01=	PGA trim mode 0 (internal input short ground).
	10=	PGA trim mode 1 (internal input shorted, external from PGAP to different common mode points).
	11=	PGA trim mode 2 (internal input shorted, external from PGAGND to different common mode points)
Bit5~Bit0	PGAADJ<5:0>:	PGA input offset trim bit.

PGAADJE Register

F52DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PGAADJE	PGAADJE7	PGAADJE6	PGAADJE5	PGAADJE4	PGAADJE3	PGAADJE2	PGAADJE1	PGAADJE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0	PGAADJE<7:0>:	Op-amp offset voltage regulation method selection.
	AAH =	Determined by PGAADJ<5:0> in the PGACON2 register.
	others=	Determined by the CONFIG-related bits.

22. OPERATION OF FLASH MEMORY

Flash memory is divided into two parts for users: program area and data area.

- The size: program area 16K*8Bit; data area 1K*8Bit.
- The program area is divided into 32 sectors, one sector contains 512 bytes; the data area is 2 sectors.

The memory is readable under normal working conditions. It can also be indirectly addressed by a special function register (SFR). There are four SFR registers for accessing program memory:

- MCTRL
- MDATA
- MADRL
- MADRH
- MLOCK

When operating the memory module interface, the MDATA register is used as a byte to hold the 8-bit data to be read/ written. While the MADR register holds the address of the accessed MDATA unit. The memory allows byte read and write, and the byte write operation writes new data (erased before writing).The write time is controlled by the on-chip timer. The on-chip charge pump generates write and erase voltages that are rated to operate within the device's voltage range for byte operations.

Since the memory type is Flash, the erase operation only supports sector erase and does not support byte erase. Before modifying the data of an address, it is recommended to save the other data, erase the current sector, and then write the data.

The memory can be read/write/erase(R/W/E) through the memory module interface.

Flash Memory Lock Register MLOCK

0xFB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MLOCK	MLOCK7	MOCK6	MLOCK5	MLOCK4	MLOCK3	MLOCK2	MLOCK1	MLOCK0
R/W	W	W	W	W	W	W	W	W
Reset value	0	1	0	1	0	1	0	1

Bit7~Bit0 MLOCK<7:0>: Memory operation enable bit.

AAH: Enable memory-related R/W/E operations

00H/FFH/55H: Disable operations

Disable writing other values

(This register only supports write operation, read as 00H)

Flash Memory Data Register MDATA

0xFE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MDATA	MDATA7	MDATA6	MDATA5	MDATA4	MDATA3	MDATA2	MDATA1	MDATA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 MDATA<7:0>: Data that is read or written to program memory

Flas Memory Low Address Register MADRL

0xFC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MADRL	MADRL7	MADRL6	MADRL5	MADRL4	MADRL3	MADRL2	MADRL1	MADRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	1	1	1	1	1

Bit7~Bit0 MADRL<7:0>: The lower 8 bits of the memory read/write operation address.

Flash Memory High Address Register MADRH

0xFD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MADRH	MADRH7	MADRH6	MADRH5	MADRH4	MADRH3	MADRH2	MADRH1	MADRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7~Bit0 MADRH<7:0>: The higher 8 bits of the memory read/write operation address.

Flash Memory Control Register MCTRL

0xFF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MCTRL	--	--	MERR	MREG	MMODE1	MMODE0	--	MSTART
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1	0	0	0	0

Bit7~Bit6 --

Bit5 MERR: Operation error flag (write 0 clear);
1= Before the programming operation, The write operation is immediately terminated when the data in the test programming address is not "FFH" (not erased).
0= ---

Bit4 MREG: Flash area selection;
1= Select data area (Low 10-bit address is valid);
0= Select program area (Low 14-bit address is valid).

Bit3~ Bit2 MMODE<1:0>: Operating mode selection:
11= Erase mode (Range of erase operation: the entire sector where the current address is located);
10= Write mode;
01= Reserved;
00= Read mode.

Bit1 Unused, read 0

Bit0 MSTART: Start operation control;
1= Start program memory R/W/E operation (Automatically cleared by hardware after the operation is completed);
0= Write: Terminate or not start program memory R/W/E operation;
Read: operation completed or operation not started.

When operating the Flash memory, the CPU is suspended, and when the operation is completed, the CPU continues to run the instruction.

6 NOP instructions must be added after the operation memory instruction:

```
MOV MCTRL,#09H          ; Write begins
NOP
NOP
NOP
NOP
NOP
NOP
MOV MCTRL,#01H          ; Read begins
NOP
NOP
NOP
NOP
NOP
NOP
```

23. UNIQUE ID (UID)

23.1 Overview

Each chip has a unique 96-digit identification number(Unique identification). It has been set at the factory and cannot be modified by the use.

23.2 UID Registers

UID0

F5E0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID0	UID7	UID6	UID5	UID4	UID3	UID2	UID1	UID0
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<7:0>

UID1

F5E1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID1	UID15	UID14	UID13	UID12	UID11	UID10	UID9	UID8
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<15:8>

UID2

F5E2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID2	UID23	UID22	UID21	UID20	UID19	UID18	UID17	UID16
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<23:16>

UID3

F5E3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID3	UID31	UID30	UID29	UID28	UID27	UID26	UID25	UID24
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<31:24>

UID4

F5E4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID4	UID39	UID38	UID37	UID36	UID35	UID34	UID33	UID32
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<39:32>

UID5

F5E5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID5	UID47	UID46	UID45	UID44	UID43	UID42	UID41	UID40
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<47:40>

UID6

F5E6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID6	UID55	UID54	UID53	UID52	UID51	UID50	UID49	UID48
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<55:48>

UID7

F5E7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID7	UID63	UID62	UID61	UID60	UID59	UID58	UID57	UID56
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<63:56>

UID8

F5E8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID8	UID71	UID70	UID69	UID68	UID67	UID66	UID65	UID64
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<71:64>

UID9

F5E9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID9	UID79	UID78	UID77	UID76	UID75	UID74	UID73	UID72
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<79:72>

UID10 (0xF5EA)

F5EAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID10	UID87	UID86	UID85	UID84	UID83	UID82	UID81	UID80
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<87:80>

UID11

F5EBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UID11	UID95	UID94	UID93	UID92	UID91	UID90	UID89	UID88
R/W	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit7~Bit0 UID<95:88>

24. TIMED WAKE UP IN SLEEP STATE

24.1 Timed Wakeup Control Registers

WUTCRH Register

0xBD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WUTCRH	WUTEN	--	WUTPS1	WUTPS0	WUTD11	WUTD10	WUTD9	WUTD8
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit7 WUTEN: Timed wake up function enable
1= Enable
0= Disable
Bit6 Not used
Bit5~Bit4 WUTPS<1:0>: Timed wake up counter clock divider.
00= F/1
01= F/8
10= F/32
11= F/256
Bit3~Bit0 WUTD<11:8>: Timed wake up time data high 4 bits

WUTCRL Register

0xBC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WUTCRL	WUTD7	WUTD6	WUTD5	WUTD4	WUTD3	WUTD2	WUTD1	WUTD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit7~Bit0 WUTD<7:0>: The lower 8 bits of the timed wake-up time data.

24.2 Timed Wake Up Principle

The internal timed wake-up principle is that after the system enters the sleep mode, the CPU and all peripheral circuits stop working, and the internal low-power oscillator LPRC starts to work, and its oscillation clock is 125KHz. Clocks are provided for the WUT (Wake Up Timer) counter.

There are two internal wake-up timing registers: WUTCRH and WUTRCL.

Bit7 of the WUTCRH register is the internal timer wake-up enable bit:

- WUTEN=1: Enable the timed wakeup function;
- WUTEN=0: Disable the timed wakeup function.

WUTCRH[3:0] and WUTCRL[7:0] form a 12-bit timer wake-up data register with a reset value of 0FFH. After entering sleep mode, the WUT counter starts timing. When the value of the WUT counter is equal to the value of the timer wake-up data register, the system oscillator is started to enter the wake-up wait state.

Timed wake up time: $T=(WUTD[11:0]+1)\times WUTPS\times T_{LSI}$

25. ELECTRICAL PARAMETERS

25.1 Absolute Maximum Rating

Symbol	Item	Min	Max	Unit
T_{ST}	storage temperature	-55	150	℃
T_A	Operating temperature	-40	105	℃
VDD-VSS	Operating voltage	-0.3	5.8	V
V_{IN}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	120	mA
I_{IO}	Single IO maximum sink current	-	50	mA
	Single IO maximum output current	-	20	mA
	All IO maximum sink current	-	120	mA
	All IO maximum output current	-	120	mA

25.2 DC Electrical Characteristics

VDD-VSS=2.1～5.5V, T_A=25℃

Symbol	Item	Test condition	Min	Typ	Max	Unit
VDD	Operating voltage	F_{SYS}=48MHz, F_{CPU}=F_{SYS}/2 F_{SYS}=8MHz~24MHz, F_{CPU}=F_{SYS}	2.1	-	5.5	V
I_{DD}	Normal mode	VDD=5V, F_{SYS}=48MHz, all peripherals OFF F_{CPU}=F_{SYS}/2	-	6	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals OFF F_{CPU}=F_{SYS}/2	-	6	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals OFF F_{CPU}=F_{SYS}	-	4	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals OFF F_{CPU}=F_{SYS}	-	4	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals OFF F_{CPU}=F_{SYS}	-	3	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals OFF F_{CPU}=F_{SYS}	-	3	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals OFF F_{CPU}=F_{SYS}	-	2	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals OFF F_{CPU}=F_{SYS}	-	2	-	mA
	IDLE mode	VDD=5V, F_{SYS}=48MHz, all peripherals OFF	-	4	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals OFF	-	4	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals OFF	-	2.5	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals OFF	-	2.5	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals OFF	-	2	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals OFF	-	2	-	mA

		VDD=5V, F_{SYS}=8MHz, all peripherals OFF	-	1.5	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals OFF	-	1.5	-	mA
I_{SLEEP1}	Sleep current	all peripherals OFF, LSE, LSE timer enable	-	20	-	uA
I_{SLEEP2}	Sleep current	all peripherals OFF, LSI, WUT timer enable	-	7	-	uA
I_{SLEEP3}	Sleep current	all peripherals OFF	-	6	-	uA
I_{LI}	Input leakage	-	-	-	0.1	uA
V_{IL}	Input low level	-	VSS	-	0.3VDD	V
V_{IH}	Input high level	-	0.7VDD	-	VDD	V
V_{OL}	Output low voltage	VDD=5V, I_{OL1}=12mA	-	-	0.4	V
		VDD=5V, I_{OL2}=7mA	-	-	0.4	V
		VDD=3V, I_{OL1}=9mA	-	-	0.4	V
		VDD=3V, I_{OL2}=5mA	-	-	0.4	V
V_{OH}	Output high voltage	VDD=5V, I_{OH1}=40mA	3.5	-	-	V
		VDD=5V, I_{OH2}=20mA	3.5	-	-	V
		VDD=3V, I_{OH1}=15mA	2.1	-	-	V
		VDD=3V, I_{OH2}=8mA	2.1	-	-	V
R_{PH}	Pull-up resistor	-	-	32	-	KΩ
R_{PL}	Pull-down resistor	-	-	32	-	KΩ

25.3 AC Electrical Parameters

25.3.1 Power-Up and Power-Down Operation

T_A=25℃, excluding 32.768K crystal oscillation start time

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
T_{RESET}	Reset time	VDD=5V	-	16	-	ms
T_{VDDR}	VDD rise rate	VDD=5V	20	-	-	us/V
T_{VDDF}	VDD fall rate	VDD=5V	20	-	-	us/V

25.3.2 External Oscillator

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{HSE}	Operating Voltage	F=8/16MHz,C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Operating Voltage	F=32.768KHz,C_{XT}=10-22pF	2.1	-	5.5	V

25.3.3 Internal Oscillator

VDD=2.1V-5.5V

Symbol	Item	Test condition	Frequency Error	Min.	Typ.	Max.	Unit
F_{HSI}	Internal high speed 48MHz	T_A=25℃	±1%	-	48	-	MHz
		T_A=-20℃ to 85℃	±2%	-	48	-	MHz
		T_A=-40℃ to 105℃	±3%	-	48	-	MHz
F_{LSI}	Internal low speed 125KHz	T_A=25℃	±5%	-	125	-	KHz
		T_A=-40℃ to 105℃	±50%	-	125	-	KHz

25.4 Low Voltage Reset Electrical Parameters

Symbol	Item	Min.	Typ.	Max.	Unit
V_{LVR1}	Low pressure detection threshold 1.8V	1.65	1.8	1.95	V
V_{LVR2}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVR3}	Low pressure detection threshold 2.5V	2.35	2.5	2.65	V
V_{LVR4}	Low pressure detection threshold 3.5V	3.3	3.5	3.65	V

25.5 LVD Electrical Characteristics

Symbol	Item	Min.	Typ.	Max.	Unit
V_{LVD1}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVD2}	Low pressure detection threshold 2.2V	2.05	2.2	2.35	V
V_{LVD3}	Low pressure detection threshold 2.4V	2.25	2.4	2.55	V
V_{LVD4}	Low pressure detection threshold 2.7V	2.55	2.7	2.85	V
V_{LVD5}	Low pressure detection threshold 3.0V	2.85	3.0	3.15	V
V_{LVD6}	Low pressure detection threshold 3.7V	3.55	3.7	3.85	V
V_{LVD7}	Low pressure detection threshold 4.0V	3.85	4.0	4.15	V
V_{LVD8}	Low pressure detection threshold 4.3V	4.15	4.3	4.45	V

25.6 ADC Electrical Characteristics

T_A=25℃

Symbol	Item	Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage	2.5	-	5.5	V
V_{REF1}	Reference voltage1	-	V_{AVDD}	-	V
V_{REF2}	Reference voltage 2 (not V_{BG})	1.185	1.2	1.215	V
V_{REF3}	Reference voltage3	1.985	2.0	2.015	V
V_{REF4}	Reference voltage4	2.385	2.4	2.415	V
V_{REF5}	Reference voltage 5	2.985	3.0	3.015	V
V_{ADI}	Input Voltage	0	-	V_{REF}	V
N_R	Resolution		12		Bit
DNL	Differential nonlinear error (V_{REF} =V_{AVDD} =5V, T_{ADCK} =0.5us)		±2		LSB
INL	Integral nonlinearity error (V_{REF} =V_{AVDD} =5V, T_{ADCK} =0.5us)		±4		LSB
T_{ADCK}	ADC clock period	0.5	-	32	us
T_{ADC}	ADC conversion time	-	18.5	-	T_{ADCK}
F_S	Sampling rate (V_{REF} =V_{AVDD} =5V)		100		Ksps

25.7 BANDGAP Electrical Characteristics

Symbol	Item	Test condition	Min.	Typ.	Max.	Unit
V_{BG}	Internal reference 1.2V	VDD=2.1-5.5V, T_A=-40℃ to 105℃	1.182	1.2	1.218	V

25.8 FLASH Electrical Characteristics

Symbol	Item	Test condition	Min.	Typ.	Max.	Unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating Temperature	-	-40	27	105	℃
$N_{ENDURANCE}$	Number of erasures	ProgramFLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	Cycle
T_{RET}	Data storage time	25℃	100	-	-	year
T_{ERASE}	Sector erase Time	-	-	1.5	-	ms
T_{PROG}	Programming time	-	-	7	-	us
I_{DD1}	Reading current	-	-	-	2.5	mA
I_{DD2}	Programming current	-	-	-	3.6	mA
I_{DD3}	Erase current	-	-	-	2	mA

25.9 OP Electrical Characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, unless otherwise stated

Symbol	Item	Test condition	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	2.5	-	5.5	V
I_Q	Static current	V_{SENSE}=0mV	-	1.0	1.6	mA
I_{SD}	Turn-off current	-	-	5	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input Characteristics						
V_{OS}	Input offset voltage	Not zeroed	-	±3.5	-	mV
		After zeroing	-	±0.5	±1.0	
V_{CM}	Common-mode input voltage range	-40℃~105℃	0	-	VDD-1.5	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
Output Characteristics						
C_{LOAD}	Capacitive load	-	-	30	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD-0.3	V
V_{OL}	Minimum output voltage	-40℃~105℃	0.3	-	-	V
Frequency Characteristics						
A_{OL}	Open-loop gain	-	-	80	-	dB
BW	Bandwidth	R_{LOAD}=2K,C_{LOAD}=100pF	-	5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	75	-	dB

CMRR	Common-mode rejection ratio	V_{IN+}=0.3~ (VDD-1.5) -40℃~105℃	-	90	-	dB
Transient Characteristics						
SR	Slew rate	R_{LOAD} =2K,C_{LOAD} =100pF	-	±8	-	V/μs
T_{STB}	Stabilization time	-	-	-	2	μs

25.10 ACMP Electrical Characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, unless otherwise stated.

Symbol	Item	Test condition	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	2.1	-	5.5	V
I_Q	Static current	V_{SENSE}=0.1V	-	0.2	0.3	mA
I_{SD}	Turn-off current	V_{SENSE}=0.1V	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input Characteristics						
V_{OS}	Input offset voltage	Not zeroed	-	±4.0	-	mV
		After zeroing	-	±0.5	±1.0	
V_{CM}	Common-mode input voltage range	-40℃~105℃	-0.1	-	VDD-1.5	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃~105℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open-loop gain	-	-	85	-	dB
BW	Bandwidth	-	-	150	-	MHz
PSRR	Power supply rejection ratio	VDD=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common-mode rejection ratio	VDD=2.1~5.5V -40℃~105℃	-	90	-	dB
Transient characteristics						
T_{STB}	Stabilization time	-	-	-	5	μs
T_{PGD}	Response delay	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

25.11 PGA Electrical Characteristics

T_A=25℃, VDD=5V, V_{IN+}=0.01V, unless otherwise stated. (G is the gain multiplier)

Symbol	Item	Test condition	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	2.5	-	5.5	V
I_Q	Static current	V_{OUT}=2V	-	0.5	0.7	mA
I_{SD}	Turn-off current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input Characteristics						
V_{OS}	Input offset voltage	Not zeroed	-	±2.5	-	mV
		After zeroing	-	±0.1	±0.2	
V_{CM}	Common-mode input voltage range	G=1	0.032	-	(VDD-1.5)/G	V
		G=2	0.016			
		G=4	0.008			
		G=8	0.004			
		G=16	0.002			
		G=32, 64,128	0.001			
I_B	Input bias current	-	-	10	-	pA
I_{OS}	Input offset current	-	-	10	-	pA
Output characteristics						
EG	Gain error	G=1, 2, 4, 8, 16	-1	-	1	%
		G=32	-2	-	2	
		G=64,128	-4	-	4	
C_{LOAD}	Capacitive load	-	-	10	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD-1.5	V
V_{OL}	Minimum output voltage	-40℃~105℃	0.032	-	-	V
Frequency characteristics						
BW	Bandwidth	C_{LOAD}=10pF,G=1	-	1.5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V,G=16	-	75	-	dB
CMRR	Common-mode rejection ratio	-40℃~105℃	-	80	-	dB
Transient characteristics						
SR	Slew rate	C_{LOAD}=10pF,G=32	-	10	-	V/μs
T_{STB}	Stabilization time	-	-	-	2	μs
$T_{SH(1)}$	Sample Hold Time	-	-	3	-	μs

Note (1): This electrical characteristic is valid when sample hold mode is selected.

25.12 EFT Electrical Characteristics

Symbol	Item	Test condition	Rating
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDDand VSSpins to induce a functional disturbance	T_A = + 25 ℃, HSI=8MHz, conforms to IEC 61000-4-4	4B

Note: Electrical fast transient pulse train (EFT) immunity performance is closely related to system design (including power supply structure, circuit design, layout and wiring, chip configuration, program structure, etc.). The EFT parameters in the above table are measured on CMS's internal testbed and are not applicable to all applications and are provided for reference only. In applications with high EFT performance requirements, care should be taken to avoid interference sources affecting system operation.

25.13 ESD Electrical Characteristics

Symbol	Item	Test condition	Grade
V_{ESD}	Electrostatic discharge (Human body discharge mode HBM)	T_A = + 25℃, JEDEC EIA/JESD22- A114	3B
	Electrostatic discharge (Machine discharge mode MM)	T_A = + 25℃, JEDEC EIA/JESD22- A115	C

25.14 Latch-Up Electrical Characteristics

Symbol	Item	Test condition	Classification
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25℃)

26. INSTRUCTION

Assembly instructions include 5 categories: Arithmetic operations, logic operations, data transfer operations, Boolean operations and program branch instructions, all of these instructions are compatible with standard 8051.

26.1 Symbol Description

Symbol	Description
Rn	Working register R0-R7
Direct	Unit address of internal data memory RAM (00H-FFH) or address in special function register SFR
@Ri	Indirect Addressing Register (@R0 or @R1)
#data	8-bit binary constants
#data16	16-bit binary constant in the instruction
Bit	Bit address in internal data memory RAM or special function register SFR
Addr16	16-bit address, address range 0-64KB
Addr11	11-bit address, address range 0-2KB
Rel	Relative Address
A	Accumulator

26.2 Instruction Set

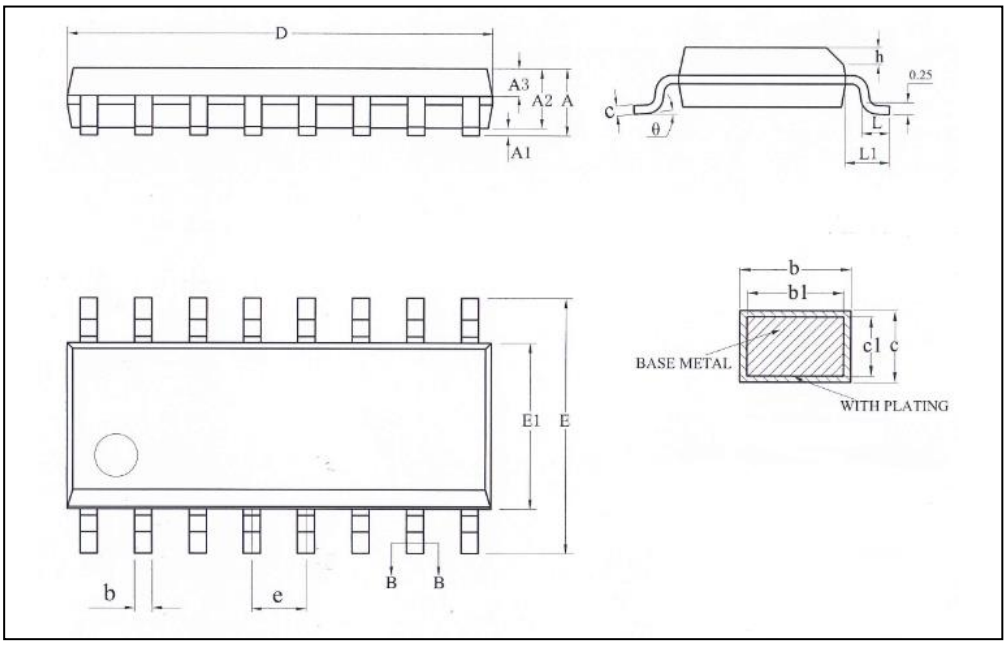
Mnemonic symbol		Description
Operation type		
ADD	A,Rn	Add register to accumulator.
ADD	A,direct	Add directly addressed data to accumulator.
ADD	A,@Ri	Add indirectly addressed data to accumulator.
ADD	A,#data	Add immediate data to accumulator.
ADDC	A,Rn	Add register to accumulate or with carry.
ADDC	A,direct	Add directly addressed data to accumulator with carry.
ADDC	A,@Ri	Add indirectly addressed data to accumulator with carry.
ADDC	A,#data	Add immediate data to accumulator with carry.
SUBB	A,Rn	Subtract register from accumulator with borrow.
SUBB	A,direct	Subtract directly addressed data from accumulate or with borrow.
SUBB	A,@Ri	Subtract in directly addressed data from accumulator with borrow.
SUBB	A,#data	Subtract immediate data from accumulate or with borrow.
INC	A	Increment accumulator.
INC	Rn	Increment register.
INC	direct	Increment directly addressed location.
INC	@Ri	Increment indirectly addressed location.
INC	DPTR	Increment data pointer.
DEC	A	Decrement accumulator.
DEC	Rn	Decrement register.
DEC	direct	Decrement directly addressed location.
DEC	@Ri	Decrement indirectly addressed location.
MUL	AB	Multiply A and B.
DIV	AB	Divide A by B.
DA	A	Decimally adjust accumulator.
Logical operation type		
ANL	A,Rn	AND register to accumulator.
ANL	A,direct	AND directly addressed data to accumulator.
ANL	A,@Ri	AND indirectly addressed data to accumulator.
ANL	A,#data	AND immediate data to accumulator.
ANL	direct,A	AND accumulator to directly addressed location.
ANL	direct,#data	AND immediate data to directly addressed location.
ORL	A,Rn	OR register to accumulator.
ORL	A, direct	OR directly addressed data to accumulator.
ORL	A,@Ri	OR indirectly addressed data to accumulator.
ORL	A, #data	OR immediate data to accumulator.
ORL	direct,A	OR accumulator to directly addressed location.
ORL	direct,#data	OR immediate data to directly addressed location.
XRL	A,Rn	Exclusive OR (XOR) register to accumulator.
XRL	A,direct	XOR directly addressed data to accumulator.
XRL	A,@Ri	XOR indirectly addressed data to accumulator.
XRL	A,#data	XOR immediate data to accumulator.
XRL	direct,A	XOR accumulator to directly addressed location.
XRL	direct,#data	XOR immediate data directly addressed location.
CLR	A	Clear accumulator.
CPL	A	Complement accumulator.

Mnemonic symbol		Description
RL	A	Rotate accumulator left.
RLC	A	Rotate accumulator left through carry.
RR	A	Rotate accumulator right.
RRC	A	Rotate accumulator right through carry.
SWAP	A	Swap nibbles within the accumulator.
Data transmission type		
MOV	A,Rn	Move register to accumulator.
MOV	A,direct	Move directly addressed data to accumulator.
MOV	A,@Ri	Move indirectly addressed data to accumulator.
MOV	A,#data	Move immediate data to accumulator.
MOV	Rn,A	Move accumulator to register.
MOV	Rn,direct	Move directly addressed data to register.
MOV	Rn,#data	Move immediate data to register.
MOV	direct,A	Move accumulator to direct.
MOV	direct,Rn	Move register to direct.
MOV	direct1,direct2	Move directly addressed data to directly addressed location.
MOV	direct,@Ri	Move indirectly addressed data to directly addressed location.
MOV	direct,#data	Move immediate data to directly addressed location.
MOV	@Ri,A	Move accumulator to indirectly addressed location.
MOV	@Ri,direct	Move directly addressed data to indirectly addressed location.
MOV	@Ri,#data	Move immediate dato to102n directly addressed location.
MOV	DPTR,#data16	Load data pointer with a 16-bitimmediate.
MOVC	A,@A+DPTR	Load accumulator with a code byte relative to DPTR.
MOVC	A,@A+PC	Load accumulator with a code byte relative to PC.
MOVX	A,@Ri	Move external RAM (8-bitaddress) to accumulator.
MOVX	A,@DPTR	Move external RAM (16-bitaddress) to accumulator.
MOVX	@Ri,A	Move accumulator to external RAM (8-bitaddress).
MOVX	@DPTR,A	Move accumulator to external RAM(16-bitaddress).
PUSH	direct	Push directly addressed data onto stack.
POP	direct	Pop directly addressed data location fromstack.
XCH	A,Rn	Exchange register with accumulator.
XCH	A, direct	Exchange directly addressed location with accumulator.
XCH	A,@Ri	Exchange indirect RAM with accumulator.
XCHD	A,@Ri	Exchange low-order nibbles of indirect and accumulator.
Boolean type		
CLR	C	Clear carry flag.
CLR	bit	Clear directly addressed bit.
SETB	C	Set carry flag.
SETB	bit	Set directly addressed bit.
CPL	C	Complement carry flag.
CPL	bit	Complement directly addressed bit.
ANL	C,bit	AND directly addressed bitto carry flag.
ANL	C,/bit	AND complement of directly addressed bit to carry.
ORL	C,bit	OR directly addressed bit to carry flag.
ORL	C,/bit	OR complement of directly addressed bit to carry.
MOV	C,bit	Move directly addressed bit to carry flag.
MOV	bit,C	Move carry flag to directly addressed bit.
Program jump type		

Mnemonic symbol		Description
ACALL	addr11	Absolute subroutine call
LCALL	addr16	Long subroutine call
RET		Return from subroutine
RETI		Return from interrupt
AJMP	addr11	Absolute jump
LJMP	addr16	Long jump
SJMP	rel	Short jump (relative address)
JMP	@A+DPTR	Jump indirect relative to the DPTR
JZ	rel	Jump if accumulator is zero
JNZ	rel	Jump if accumulator is not zero
JC	rel	Jump if carry flag is set
JNC	rel	Jump if carry flag is not set
JB	bit,rel	Jump if directly addressed bit is set
JNB	bit,rel	Jump if directly addressed bit is not set
JBC	bit,rel	Jump if directly addressed bit is set and clear bit
CJNE	A,direct,rel	Compare directly addressed data to accumulator and jump if not equal
CJNE	A,#data,rel	Compare immediate data to accumulator and jump if not equal
CJNE	Rn,#data,rel	Compare immediate data to register and jump if not equal
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal
DJNZ	Rn,rel	Decrement register and jump if not zero
DJNZ	direct,rel	Decrement directly addressed lacation and jump if not zero
NOP		No operation for one cycle
Read-modify-write instruction (Read-Modify-Write)		
ANL		Logical AND. (ANL direct, A and ANL direct, #data)
ORL		Logical OR. (ORL direct, A and ORL direct, #data)
XRL		Logical exclusive OR. (XRL direct, A and XRL direct, #data)
JBC		Jump if bit = 1 and clear it. (JBC bit, rel)
CPL		Complement bit. (CPL bit)
INC		Increment. (INC direct)
DEC		Decrement. (DEC direct)
DJNZ		Decrement and jump if not zero. (DJNZ direct, rel)
MOV	bit,C	Move carry to bit. (MOV bit, C)
CLR	bit	Clear bit. (CLR bit)
SETB	bit	Set bit. (SETB bit)

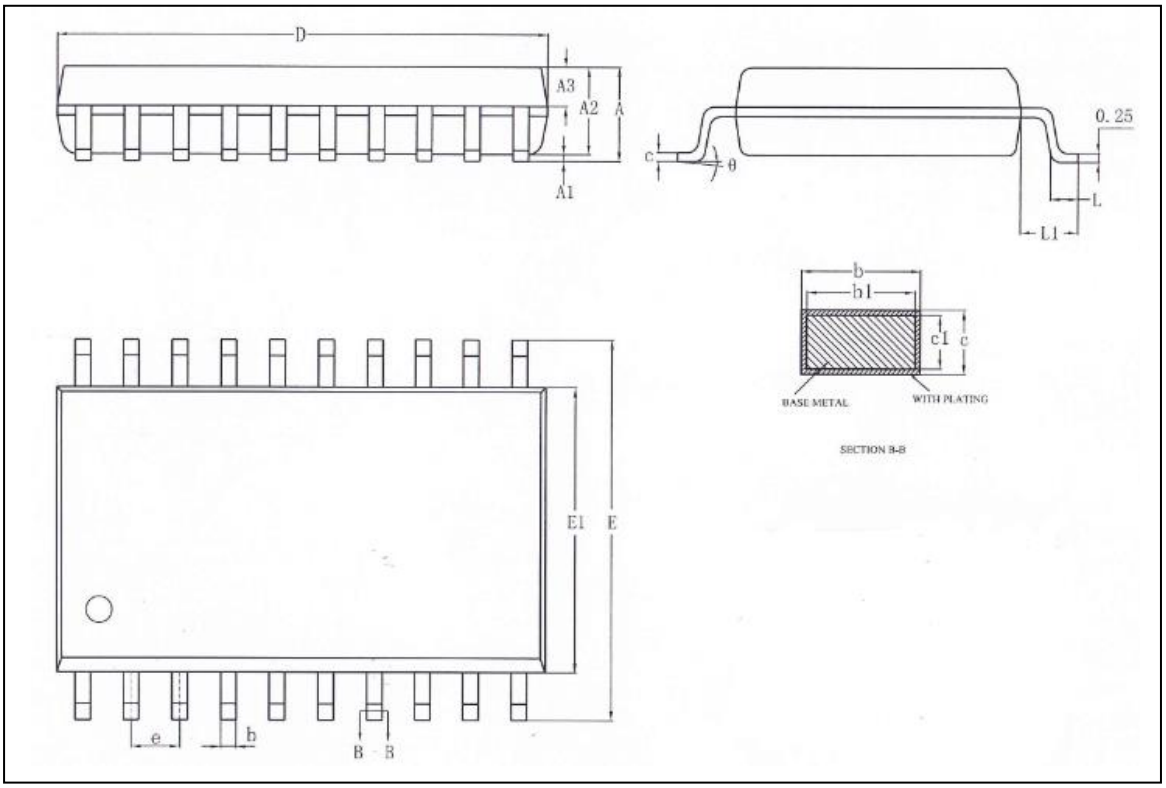
27. PACKAGE

27.1 SOP16



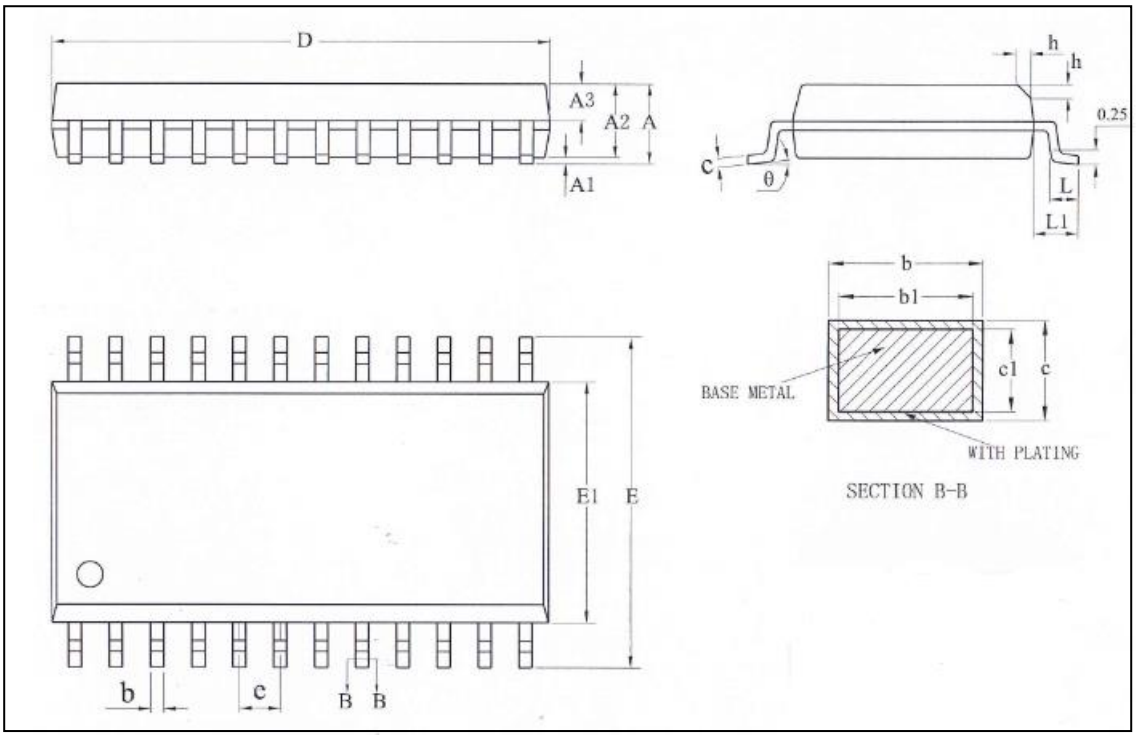
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

27.2 SOP20



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	12.70	12.80	12.90
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
θ	0	-	8°

27.3 SOP24



Symbol	Millimeter		
	Min	Nom	Max
A	2.36	2.54	2.64
A1	0.10	0.20	0.30
A2	2.26	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	15.30	15.40	15.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
h	0.25	-	0.75
θ	0	-	8°

28. REVISION HISTORY

Version	Date	Revised content
V1.0	November 2019	Initial Version
V1.01	March 2020	Modified the timer 3/4 description. Modified the ADC register description. Modified the ACMP structure block diagram. Corrected some errors in the package diagram. Updated manual format
V1.10	November 2021	Updated font format Modified the contents of the flash memory operation
V1.11	April 2022	Removed ADC clock frequency example, adjusted I2C description, removed FLASH operation time related description, adjusted port multiplexing function description, added BUZZER notes, changed some register bit description, optimized some text expression
V1.12	August 2022	Added AD channel description to CMS80F2313 pin diagram
V1.13	April 2023	1) Corrected some information in 27.2 Package Size. 2) Updated 25.12 EFT Electrical Characteristics, 25.13 ESD Electrical Characteristics, 25.14 Latch-Up Electrical Characteristics. 3) Modified some parameters in 25.3.3 Internal oscillator. 4) Corrected some parameters in 25.3.1 Power-Up and Power-Down Operation.